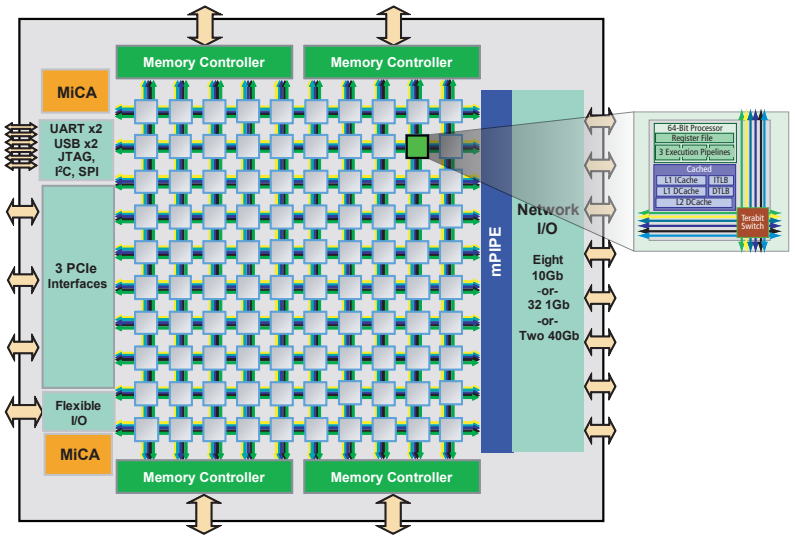
TILE-Gx™ Processor Family

Product Brief

Overview

The TILE-Gx™ processor family processor brings 64-bit multicore computing to the next level, enabling a wide range of applications to achieve the highest performance in the market. This latest-generation processor family features devices with 16 to 100 identical processor cores (tiles) interconnected with Tilera's iMesh™ on-chip network. Each tile consists of a complete, full-featured processor as well as L1 and L2 cache and a non-blocking switch that connects the tiles into the mesh. As with all Tilera processors, each tile can independently run a full operating system, or a group of multiple tiles can run a multi-processing OS, like SMP Linux.



The TILE-Gx family processor slashes board real estate requirements and system costs by integrating a complete set of memory and I/O controllers, which eliminates the need for an external north bridge or south bridge. TileDirect™ technology provides coherent I/O directly into the tile caches to deliver ultimate low-latency packet processing performance. Tilera's Dynamic Distributed Cache (DDC™) system for fully coherent cache across the tile array enables scalable performance for threaded and shared memory applications.

The TILE-Gx processors are programmed in ANSI standard C and C++, enabling developers to leverage their existing software investment. Tiles can be grouped in clusters to apply the appropriate amount of horsepower to each application. Since multiple virtualized operating system instances can be run on the TILE-Gx simultaneously, it can replace multiple CPU and DSP subsystems for both the data plane and control plane.

	Features	Enables
Massively Scalable	• Array of 16 to 100 general purpose processor cores (tiles) • 64-bit VLIW processors with 64-bit instruction bundle • Three-deep pipeline with up to 3 instructions per cycle • Massive 32 Mbytes of on-chip cache in the TILE-Gx100 • Up to 750 billion 32-bit operations per second (BOPS) • Up to 200 • of on-chip mesh interconnect • Over 500 Gbps memory bandwidth with two or four 64-bit DDR3 controllers	• 40 - 80 Gbps of Snort® IPS scanning • 60 - 80 Gbps nProbe • 80 Gbps Fast IP forwarding • H.264 HD encode for dozens of streams of 1080p (baseline profile) • 64+ channels of OFDM baseband processing
Power Efficiency	• 1.0 to 1.5GHz operating frequency • 10W to 55W for typical applications • Idle tiles can be put into low-power sleep mode	• Highest performance per watt • Simple thermal management and power supply design • Small system form factor
Integrated Solution	• Four 64-bit DDR3 memory controllers with optional ECC • Up to eight 10GbE XAUI interfaces and two Interlaken interfaces • Three Gen2 PCIe interfaces, each selectable as endpoint or root complex • Up to 32 GbE MAC interfaces • Wire-speed mPIPE™ packet processing engine	• Reduces BOM cost – standard interfaces on-chip • Dramatically reduced board real estate • Up to 80 Gbps of PCIe bandwidth • Over 80 Gbps of packet I/O bandwidth • Up to 40 Gbps VPN performance
Multicore Development Environment Options	• ANSI standard C/C++ compiler • Advanced profiling and debugging designed for multicore programming • Supports SMP Linux and virtualization • Tilera Multicore Component (TMC™) libraries for efficient inter-tile communication	• Runs off-the-shelf C/C++ programs • Reduces debug and optimization time • Enables faster time to production code • Uses standard multicore communication mechanisms

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Features

64-bit processor cores: Each of the 16 to 100 cores is a full 64-bit computing engine with 64-entry register file. The processors include rich DSP and SIMD extensions, enabling both general-purpose and multimedia processing in the same device.

Scalable cache: The cores include 32KB L1i, 32KB L1d, and 256KB L2 cache. With its peer-to-peer coherency, the powerful DDC system scales easily to the 100-core level and beyond.

Wire-speed packet engine: Tilera's new mPIPE™ (multicore Programmable Intelligent Packet Engine) delivers user-programmable flexibility to the integrated network I/O system. Up to 120 Mpps of packet classification, load balancing, and buffer management is delivered by this engine.

Hardware encryption and compression: The TILE-Gx family incorporates the revolutionary MiCA™ (Multistream iMesh Crypto Accelerator) engine that includes a robust set of encryption, hashing, and public key operations at speeds to 40Gbps and 50,000 RSA operations per second.

Development Environment

Tilera's Multicore Development Environment™ (MDE) is a complete standards-based multicore programming solution that enables developers to take full advantage of the parallel processing potential of the Tile Processor™ architecture.

Leveraging Open Source software and the developer's existing software code base achieves impressive results in an extremely short period of time. As developers become more familiar with large-scale multicore, they can capitalize on enhanced tools and libraries offered in the MDE.

Tilera's MDE includes:

- Standard Eclipse-based IDE
- GCC compiler (ANSI C/C++)
- Multi-tile, timing-accurate simulator
- Whole chip debug and performance analysis
- Line-by-line profiling
- Full SMP Linux support
- TMC libraries for efficient inter-communication

Target Applications

The TILE-Gx family of processors has the flexibility, performance and power efficiency to support a wide range of computing applications, including advanced networking, digital multimedia, wireless infrastructure, and cloud computing. Because it is a general-purpose multicore processor, the TILE-Gx can run multiple operating systems and applications simultaneously. The combination of the virtual memory, I/O with multi-protection levels, and Tilera's Multicore Hardwall™ technology provides protection for multiple OS and application instances.

Intelligent Networking Products

- Firewall and VPN
- Intrusion Detection/Prevention (IDS/IPS)
- Unified Threat Management (UTM)
- L4-7 Deep Packet Inspection (DPI)
- Network Monitoring and Forensics

Wireless Infrastructure (GSM, WiMAX, LTE)

- Base Transceiver Station (BTS)
- Base Station Controller (BSC)
- Wireless Backbone Gateways (GGSN and SGSN)
- Audio/Video Media Gateway

Digital Multimedia Products

- Video Transcoding/Transrating
- Videoconferencing MCU and Endpoints
- Streaming IPTV and Video-on-Demand
- Video Post-Production Processing

Cloud Computing

- Web Applications (LAMP)
- Data caching (Memcached)
- Databases

TILE-Gx Family Specifications

Device	Number of Tiles	Packet Interfaces	Interlaken Interfaces	PCIe Interfaces (Gen 2)	DDR3 Memory	Processor Frequencies	Package
TILE-Gx100™	100	8 XAUI, 32 SGMII	2x 40G	Two 8-lane, one 4-lane	4x @ 2133	1.25, 1.5GHz	45 x 45mm BGA
TILE-Gx64™	64	6 XAUI, 24 SGMII	2x 40G	Two 8-lane, one 4-lane	4x @ 1600	1.25, 1.5GHz	45 x 45mm BGA
TILE-Gx36™	36	4 XAUI, 16 SGMII	–	One 8-lane, two 4-lane	2x @ 1600	1.25, 1.5GHz	35 x 35mm BGA
TILE-Gx16™	16	1 XAUI, 12 SGMII	–	Three 4-lane	2x @ 1333	1.0, 1.25GHz	35 x 35mm BGA

For more information on Tilera products, visit www.tilera.com