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Assemblyman Reed Gusciora, Stephanie Harris, Coalition for Peace Action, and New Jersey Peace Action, Plaintiffs, v. Jon Corzine, Governor of the State of New Jersey (in his official capacity) and Nina Mitchell Wells, Secretary of State of the State of New Jersey (in her official capacity), Defendants.	SUPERIOR COURT LAW DIVISION MERCER COUNTY Docket No. MER-L-2691-04 CIVIL ACTION

EXPERT REPORT OF WAYNE WOLF ON FAKE Z80s

INTRODUCTION

1. My name is Wayne Hendrix Wolf. My CV is attached as Exhibit A. I am Professor, Rhesa "Ray" S. Farmer, Jr., Distinguished Chair of Embedded Computing Systems and Georgia Research Alliance Eminent Scholar at the Georgia Institute of Technology (Georgia Tech). I hold B. S., M. S. and Ph. D. degrees in electrical engineering from Stanford University. Before joining Georgia Tech, I was on the faculty of Princeton University from 1989 to 2007. I was a New Jersey resident for more than 20 years.

2. I have served as an expert witness in several patent lawsuits. I give a partial list in Exhibit B and will complete this list before my deposition. I have testified and/or been deposed in Federal District courts in Portland and San Francisco on several cases between Quickturn, Mentor Graphics, and Aptix which involved FPGA-based emulators; I have been deposed for the Federal District Court of Delaware for WABTEC on train airbrake design; most recently, I testified last fall in Federal District Court in the District of Columbia for a number of camera manufacturers. I have also testified on two occasions at the International

Trade Commission about the Quickturn/Mentor Graphics matters.

3. I am an author or co-author of well over 200 technical publications, including a great deal of work published over the past 25 years on microprocessors, embedded software, logic design, and field-programmable gate array systems. I have published research on embedded system security. I helped to create a workshop on embedded system security. I have also published extensively in video processing and computer vision. All such work is directly relevant to my report and testimony. These publications include several books. I believe that three of them are most relevant to this report: *Modern VLSI Design* [Wol09], *FPGA-Based System Design* [Wol04]; and *Computers as Components* [Wol08]. PowerPoint presentations derived from these books are available at http://www.waynewolf.us. I have relied on my research and educational experience in the preparation of this report.

4. I have also relied on my experience in FPGA-based system design thanks to my role as chairman of Verificon Corporation. I was lead designer on a real-time computer vision system implemented on a Xilinx

Virtex-II Pro FPGA. As part of this project, I supervised Verificon employees and consultants as well as my Princeton Ph.D. student Jason Schlessman. I also worked with software and hardware designers at Verificon's partner, Yokogawa Electric.

5. I have been retained by the plaintiffs in this case to render an opinion on the feasibility of creating what I will call a "Fake Z80", a modified microprocessor that can be used to change election-related data on a voting machine. I have also been retained by the plaintiffs to evaluate and comment on countermeasures proposed by the defendants to detect the Fake Z80 and its associated software. I am working on this matter pro bono.

6. A variety of methods can be used to introduce Fake Z80s into large numbers of voting machines and to use these Fake Z80s to execute software that would subvert elections. I will discuss two attack techniques of increasing levels of sophistication. Both techniques are straightforward for an attacker to conceive of and to implement. Each technique is harder to detect than the last. Overall, subverting election machine

behavior using Fake Z80s is easy and cheap to do while detecting these methods is difficult and expensive.

7. This report is dedicated to a detailed explanation of my opinions and their bases, including the definition of a variety of terms. Sequoia's October 2 rebuttal report states on p. 9, referring to previous reports on the feasibility of fake processors, "Frankly, the entire section is a fantasy." I quote from the testimony of Edwin B. Smith, March 19, 2009 (R. at 141:3-6.):

> "Q: You've testified today and written in your report that making a fake z80 chip is a fantasy and pure science fiction, correct?
>
> "A: Yes, that's in the report."

I also quote from the testimony of Michael I. Shamos, March 25, 2009 (R. at 93:7-95:10.):

> "Q: Do you know of anyone that has created a z80 processor chip that can steal votes?
>
> "A: [. . .] I think you're talking about a fraudulent z80 chip.
>
> "Q: Yes.
>
> "A: No one has demonstrated that a fraudulent z80 chip could successfully masquerade as a z80. There's no question that on a red board in a

laboratory, you can construct a simulator for a z80 that will not behave as a z80. That is correct.

"Q: Would this be something easy to accomplish?

"A: [. . .] I mean, it's hypothetically possible. But I haven't considered it a legitimate risk.

[. . .]

"THE COURT: So you don't perceive that as a risk?

"THE WITNESS: I don't perceive it as a risk worth worrying about."

Unfortunately, in my professional opinion it is all too easy for an attacker to create such a Fake Z80. The Fake Z80 is neither fantasy nor science fiction and is a very real risk that the Court should worry about a great deal. I and many of my colleagues in industry, government, and academia are very concerned about the threat posed by modified computers to a wide variety of computer systems.

8. So that the reader has a point of reference while reading my opinion, I have created a chart that summarizes my opinions on the techniques that can be used to create Fake Z80s that can be used to alter election results:

	Skill required	Time required	Cost per unit for 500 units	Cost per unit for 10,000 units
Bare FPGA repackaged in DIP	Logic design (college junior)	56 hours	$70	$70
VLSI	VLSI design (college senior/master's)	1000 hours	$640	$80

9. This report considers practitioners in three related but distinct arts: logic design, VLSI design, and embedded computing. By logic design, I mean general logic design as would be understood by computer engineers, targeting field-programmable gate arrays (FPGAs), programmable logic devices (PLDs), etc. The primary medium for logic design today would be hardware description languages (HDLs), though some designers may still prefer schematic diagrams. By VLSI design, I mean semicustom or custom design involving circuit and layout design of integrated circuits as well as logic design. By embedded computing, I mean the use of programmable computers in application-specific systems.

FPGA TECHNOLOGY

10. Mr. Terwilliger's report of February 19 states that FPGAs do not have enough memory to hold all the software required to control the subversive behavior

of the Fake Z80. He does so to claim that an FPGA with the required amount of memory would be very expensive and that relatively few models with enough memory are available. However, Mr. Terwilliger makes several misstatements about FPGAs as well as an incorrect estimate of the amount of software that needs to be stored on the FPGA. FPGAs with the required memory are much cheaper and plentiful than Mr. Terwilliger allows.

11. Specifically, Mr. Terwilliger makes four incorrect statements about these matters:

- Mr. Terwilliger states that semiconductor memory is implemented in logic gates, whereas it is in fact implemented with specialized circuits.
- Mr. Terwilliger states on page 6 of his February 19 report that "The basic unit of capacity for an FPGA is a 'gate'" whereas Xilinx FPGAs use static CMOS configuration latches to implement their logic gates. That SRAM can also be used directly as memory.
- Mr. Terwilliger believes that most FPGAs have a limited amount of memory, whereas many FPGAs have large amounts of on-chip memory.
- Mr. Terwilliger believes that an attacker would have to store both unmodified and modified software in the FPGA, whereas not all of the voting machine memory contents would have to be resident on the chip.

12. The two major types of volatile semiconductor memory are dynamic random access memory (DRAM) and static

random access memory (SRAM). SRAM generally uses a six-transistor circuit (cell) to store one bit of memory, though five-transistor cells are also known. The DRAM cell consists of a transistor and a storage capacitor.

13. Mr. Terwilliger states on page 6 of his February 19 report that "The basic unit of capacity for an FPGA is a 'gate'" but FPGAs such as Xilinx implement logic gates using lookup tables. These lookup tables are in turn implemented using static CMOS configuration latches (CCLs). For example, a 4-input gate in one of these FPGAs would be implemented as a 16-bit table. These tables can be used directly as memory rather than as logic. Any count of the available memory in an FPGA that ignores this source of RAM is therefore low.

14. Modern FPGAs provide designers with a great deal of available memory. In addition to RAM, some FPGAs also supply on-board flash. Consider, for example, the Spartan-3AN FPGA family from Xilinx [Xil08]. The XC3S200AN has 288K bits of block RAM and 28K bits of distributed RAM as well as 4M bits of in-system flash.

15. Mr. Terwilliger seriously overestimates the amount of memory required to subvert the voting machine's

software using the Fake Z80. If an attacker modifies only a portion of a voting machine's firmware, the Fake Z80 could be created so that only the modified sections of memory are stored on the Fake Z80 chip. This means that only a small amount of memory is required on the FPGA to store the malware. Many inexpensive FPGAs have the required amount of memory.

FAKE Z80 DESIGN

16. An attacker could very easily design and build a Fake Z80 that could be used to subvert the behavior of AVC Advantage voting machines. An attacker with skills in logic design could complete the design of the Fake Z80 by himself or herself. An attacker could also find thousands of people around the world who could perform this work, *without those people knowing the intended use of the device they were designing.*

17. An attacker must first design the logic for the Fake Z80 and then embody that logic in either an FPGA or a VLSI chip. The design of the Fake Z80 is very simple because designs for real Z80s are freely available on the Internet. Mr. Terwilliger, in his January 9 deposition (pp. 80-81), when asked:

> Are you familiar with Dr. Appel's assertion that a fraudulent or fake Z80 chip that does not follow legitimate firmware instruction could be installed on to the Advantage?

replied

> "Frankly, it sounds like science fiction."

As discussed elsewhere in this report, Mr. Terwilliger's views are shared by Mr. Smith and Dr. Shamos. Unfortunately, because Z80 logic designs are so easy to find and the necessary logic design skills are held by so many people, the threat of Fake Z80s is very real.

18. Logic design is a skill held by many practitioners. These skills may be acquired at universities in various departments, depending on how fields and courses are arranged at the institution. Computer engineering, electrical engineering, or computer science departments could address the relevant skills. I would expect that the holder of a bachelor's degree in the appropriate subject from a top 50 engineering school who has graduated within the past 10 years should have the relevant skills. I would expect that in the neighborhood of 10,000 practitioners in the

United States would meet the test of having ordinary skill in this art.

19. While at Princeton, I created in the 1990s the course ELE 375, Computing Structures, which continues to be taught. This is an undergraduate course normally taken in the junior year. As part of their work in this course, students designed and implemented a PDP-8 computer in Xilinx FPGAs. The PDP-8 is computer that is similar in complexity to the Z80. Students who entered this course had taken only one prior course in logic design and had limited experience in hardware description languages or computer organization. They designed the PDP-8 from scratch during a 12-week semester. Many other universities in the U. S. teach classes that train students in logic design and computer organization and would provide excellent training for the Fake Z80 attack.

20. Embedded computing is a skill held by many practitioners. The use of a Z80 to build a voting machine is an example of embedded computing. Courses in microprocessor-based system design and embedded computing are widely taught in universities. As I noted in my embedded computing column in *IEEE Computer*

magazine [Wol06], at least a half million practitioners worldwide have basic skills in embedded software design.

21. I created embedded computing courses at both Princeton and Georgia Tech. Similar courses are taught at many U. S. universities. These courses are typically taken by juniors. Students who complete one of these courses would be well versed in the fundamentals of both the hardware and software aspects of embedded computing systems. Such skills would help the attacker in the hardware and software aspects of using Fake Z80s to subvert AVC Advantage voting machines.

22. A Fake Z80 can be created by starting with an existing Z80 design and making a few small changes to that design. I believe that the changes required to build a Fake Z80 to execute the attacker's code at the proper time during operation are small and within the competence of someone of ordinary skill in the art of logic design.

23. I have studied the tv80, an open source Z80 implementation coded in the Verilog hardware description language. I obtained this code over the Internet from opencores.org. Based on my analysis, I

estimate that someone of ordinary skill in the art could create a Fake Z80, implemented in an FPGA, in 56 hours: 24 for HDL design, 16 hours for functional verification, 8 hours for FPGA implementation, and 8 hours for implementation verification. I believe that one of my ELE 375 students could do the job in considerably less time.

PACKAGED AND BARE FPGAS IN DIPS

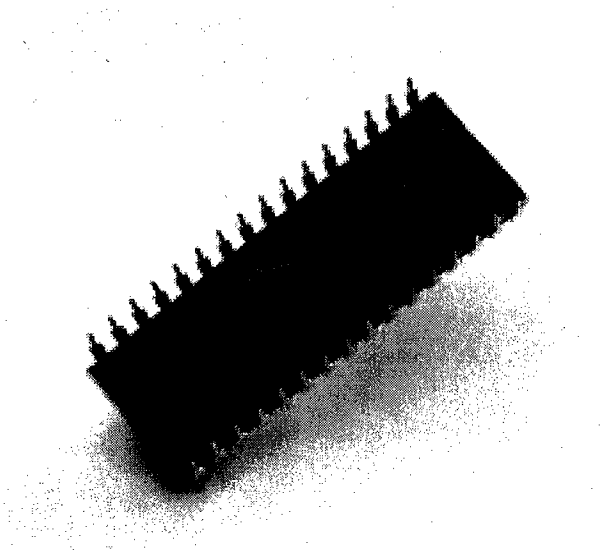
24. The completed logic design for the Fake Z80 could be embodied in a field-programmable gate array (FPGA) for insertion into AVC Advantage voting machines. The design times that I quoted in the last section include the time required to map the logic design into the chosen FPGA.

25. My design estimates lead me to conclude that the Xilinx XC3S200AN-4FTG256C part has more than enough logic and memory capacity to embody the Fake Z80 and the modified software needed to corrupt election results.

26. I checked the price of Xilinx Spartan-3AN parts on Sunday, April 5, 2009, at the DigiKey Web site (http://www.digikey.com). They quoted a price of $15.84 for the XC3S200AN-4FTG256C. I believe that quantity

discounts would be available to further reduce this price.

27. Integrated circuits (chips) are too fragile to be used as-is. We therefore put them in packages that make them easier to handle. One such package is the dual inline package (DIP). Here is a photo of a DIP, taken from my book *Modern VLSI Design*:



The DIP takes its name from the two rows of pins along the sides of the package. These pins would connect to the motherboard of the AVC Advantage. Inside the package, the pins are electrically connected to the proper points of the chip. DIPs may be made of different materials, such as ceramic or plastic. Packaging materials differ in their cost, resistance

to environmental chemicals, and thermal characteristics.

28. These FPGAs would have to be repackaged to appear as real Z80s on the motherboard. I believe that an attacker could remove the chip from its original package and repackage this "bare" FPGA to conform to the real Z80's packaging. The same technology used for delidding is one candidate for removing the FPGA from its original packaging.

29. I discussed the cost of packaging with Lee Matheson, Quality Assurance Manager at Lansdale Semiconductor. He told me that the cost of packaging a chip in a ceramic package $55/each while the cost of packaging in a plastic package is $8/each.

30. Based on the cost of purchasing FPGAs and repackaging them, I estimate the cost of an FPGA-based Fake Z80 in a ceramic package to be approximately $70.

VLSI FAKE Z80

31. An attacker could also design a VLSI Fake Z80, by which I mean a semicustom or custom integrated circuit. Designing and manufacturing the VLSI Fake Z80 is reasonable in terms of time and costs $80 per chip

to supply a Fake Z80 for every AVC Advantage machine used for voting in New Jersey. As I recall from my many years in New Jersey, this amount is small compared to the amount of money spent in many New Jersey election campaigns.

32. VLSI design is a more refined art than logic design but I would expect that graduates of top 50 engineering programs would be able to acquire those skills if they so desire. I would expect that thousands of people in the United States would be of ordinary skill in this art, at least for the level of skill required to design the chips at issue here.

33. While at Princeton, I taught ELE 462, Design of VLSI Systems. This course was often taken by seniors as well as beginning graduate students. In this course, students designed a semicustom or custom VLSI integrated circuit, including logic design, circuit design, layout, and verification.

34. Logic design and VLSI design are practiced in other countries outside the United States. For example, I have received many messages from instructors at small schools in India requesting information or help with my book *Modern VLSI Design*. As you can see from my CV,

that book has been translated into Chinese. I would expect that thousands of designers in foreign countries would have skills in logic design or VLSI design.

35. An attacker who wanted to build a VLSI Fake Z80 would start with the HDL design of the Fake Z80, such as a modified tv80. The attacker would then use computer-aided design (CAD) tools to build and verify the VLSI implementation. I believe that this task could be accomplished in about 1000 hours, or about 6 months of 8-hour days. This task could reasonably be accomplished by a single person with the appropriate skills.

36. In order to fit the additional logic and memory required for the Fake Z80 onto the same size chip, the attacker simply designs the Fake Z80 in a manufacturing process that uses smaller transistors than those used by the Zilog part. The Zilog Z80 is a very old part. We have much more advanced manufacturing technologies that are available at very reasonable costs. An attacker could put a large amount of extra logic on the same size die without any trouble.

37. The designer of a VLSI Fake Z80 could make it look like a real Z80 *even after delidding* by putting a fake top layer on the chip. This fake layer would be identical in appearance to that of the Zilog part but would be non-functional. The Fake Z80 designer would simply need to connect the pads on the fake layer to the real pads below to make the connections to the package; this is simple to do. One could not detect the addition of the extra layer by measuring the height of the chip because each layer is only a few microns thick.

38. I also discussed the cost of manufacturing Z80-style chips with Mr. Matheson of Lansdale Semiconductor. The one-time, non-recurring engineering (NRE) costs would total approximately $140,000. The actual chip fabrication for 10,000 units would be just under $100,000, based on a cost of $2000 per wafer. The cost of putting each chip in a ceramic package is $55/ea while the cost of a plastic package is $8/ea. This would come to $79 per chip for a ceramic package; let's use the figure of $80/ea for simplicity. If the attacker wanted to create only 500 VLSI Fake Z80s, the cost per chip would be $631, which we will round up to

$640. Since the incremental costs of extra chips does not require additional NRE costs, an attacker could easily scale up his or her attacks beyond New Jersey. An attacker could recoup some of his or her costs by selling additional Fake Z80s, either on the open market without disclosing its Fake Z80 attributes or directly to others who wish to subvert other devices that use Z80s.

COUNTERMEASURES PROPOSED BY DEFENDANTS

39. Defense witnesses Mr. Smith and Mr. Terwilliger have proposed several countermeasures to detect Fake Z80s: visual inspection of the printed circuit board; x-raying of the printed circuit board and/or purported Zilog Z80 part; delidding and of the purported Zilog part and visually inspecting the chip within the package; and analysis of radio frequency emissions.

Problems with all of defendants' countermeasures

40. Mr. Smith and Mr. Terwilliger's discussion of both X-raying and delidding has implicitly assumed that all the Zilog parts used in all the extant voting machines in New Jersey are the same. That assumption may not be true and needs to be verified before these countermeasures can be trusted. If there is more

than one type of real Z80 part in the field, then X-raying and delidding are likely to lead to a large number of false positives that would make inspections much more expensive and time-consuming.

41. Semiconductor manufacturers like Zilog may modify parts for a number of reasons. They may, for example, change the layout to fix bugs or to improve their manufacturing yield. As part of this work, they may modify the top layer of the chip.

42. Semiconductor manufacturers may also redesign the part for a new manufacturing process. The semiconductor industry has steadily increased the number of transistors on a chip for decades. Redesigning a chip for a new process can make the chip much smaller and cheaper to produce. This cost-reduced chip could have been put in the same package by the manufacturer. Unfortunately, x-raying or delidding would indicate that the chip was a different size and had a different set of features visible on the exposed chip, causing an inspector to erroneously flag a voting machine as having been tampered. These false positives would make the inspection process both more expensive and time-consuming.

43. Dr. Appel's report indicates that the AVC Advantage has gone through software revisions, which is to be expected. I have seen no indication of the types of records that exist about any revisions or maintenance to the hardware. In order for x-raying and delidding results to be cost-effective and reliable, a careful audit would have to be made of the board revisions and the Zilog Z80 parts used to stuff those boards.

Visual inspection of the motherboard

44. Visual inspection requires removing the circuitboard from the voting machine. The board would have to be replaced in the machine after visual inspection. This requires time and effort that increases the cost of the task. As I know from personal experience, every time one removes a board from a machine, one runs the risk of damaging the board and/or its associated connectors.

45. Visual inspection would not catch any device that had been put in a conforming DIP package. Visual inspection of the motherboard is not an effective countermeasure for either the repackaged FPGA or VLSI Fake Z80 implementations that I have discussed above.

X-ray

46. Slide 3 of Mr. Smith's PowerPoint presentation shows two X-rays with the caption "One of the FPGAs and the Z80 silicon under X-Ray Note the size difference in the silicon." These X-ray images are misleading because most of what they show is the leads that connect to the chip. The sunburst pattern around each of the chips is the set of leads that go from the bonding wires out to the pads. The defendants chose to compare two packages of different size and shape. Therefore, simple visual inspection would show that the packages are different and X-ray analysis would not be necessary. The chips are near the middle of each of these lead sets; the figure does show the dimensions of each of the chips: 0.121" x 0.145" for one and 0.143" x 0.159" for the other. The inspector needs to compare the size of the chip under inspection to the size of the chip that should be installed. Note that each of the chips is embedded in a larger gray field, making it harder for an inspector to determine the size of the chip. The inspection proposed by the defendants is considerably more subtle than, for example, testing whether a manufacturer simply failed to put any chip into a package. I have seen no

testimony as to the time and cost required to perform the required X-ray inspection at an acceptable error rate.

47. X-ray analysis cannot determine any details of the circuitry on the chip. It might not detect an FPGA that had been removed from its original package and repackaged if the FPGA were close enough in size to the real Z80. Given the advances in semiconductor technology and the FPGA manufacturers' interest in producing low cost (and therefore small) parts, we cannot dismiss the possibility out of hand such an FPGA is commercially available.

48. X-ray analysis requires not only that the motherboard be removed, but that the board also be sent to a facility for X-raying. I discussed the difficulties and risks of removing and replacing the circuitboard in paragraph 44. Those same difficulties and risks are also involved when the motherboard is removed and replaced.

49. X-ray analysis could not identify a VLSI Fake Z80 that was the same physical size and shape as the real Z80 that should have been installed in the machine.

Delidding

50. Delidding and visual inspection of the chip inside the package would identify FPGAs. It would not identify a VLSI Fake Z80 that was the same physical size and shape as the proper Z80 and had a decoy top layer conforming to the real Z80's appearance. As I discussed above, an attacker can easily make a VLSI Fake Z80 that would evade detection by delidding.

51. Delidding requires not only that the motherboard be removed, but that the board also be sent to a facility for removal of the chip and its delidding. I discussed the difficulties and risks of removing and replacing the motherboard in paragraph 48.

Radio frequency analysis

52. Analysis of radio frequency (RF) emissions from the voting machine has been proposed as a countermeasure to the use of Fake Z80s. RF analysis as a means of detecting Fake Z80s would require a great deal of experimentation and may not work. As a result, this countermeasure is highly speculative. One difficulty is that signatures would have to be found that could distinguish between modified and unmodified voting machine behavior.

53. But a more fundamental concern with RF emissions analysis is making the RF measurements themselves. The Federal Communications Commission (FCC) regulates the amount of electromagnetic interference (EMI) that can be generated by devices. Many devices therefore use shielding to prevent radio frequencies from leaving the device. The metal casing that encloses the Z80 motherboard is not only used to physically enclose the motherboard. It is a Faraday cage, a physics term for a closed electromagnetic shield. (In fact, I suspect that it is primarily an RF shield and its anti-tamper role is secondary.) I believe that any radio antenna used to pick up RF emissions for analysis would have to be placed within the metal casing. If the seals had to be removed and replaced, the time and cost of this countermeasure would be much higher.

CONCLUSIONS

54. In summary, a series of technical advances have made the design and manufacturing of Fake Z80s well within the means of attackers. When I was an undergraduate at Stanford, the Z80 was a state-of-the-art chip. Today, it is a well-understood and easily replicated technology. The logic design of a Fake Z80 would start

from Z80 designs available over the Internet and could be completed in less than two weeks' time. Inexpensive FPGAs could be used to embody the Fake Z80 and these Fake Z80 FPGAs could be packaged to evade visual inspection of the motherboard. An attacker could build a VLSI Fake Z80 with a fake top layer that would evade visual checking of the chip even after delidding. Methods for checking for Fake Z80s are not feasible or cost-effective. They require significant manipulation of the machine, which costs time and money. These manipulations also risk breaking the voting machines.

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Wayne Wolf

Dated: April 7, 2009
Atlanta, Georgia

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Deposition testimony, Paul Terwilliger, January 9, 2009.

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Expert Report of Dr. Andrew Appel, August 28, 2008.

EXHIBIT A

Wayne Hendrix Wolf

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Personal Information

Date of Birth August 12, 1958 in Washington, D. C.

Citizenship USA.

Telephone *voice* (404) 228 5767; *fax* (404) 228 8203.

Education

April, 1984 *Doctor of Philosophy, Electrical Engineering, Stanford University*. Thesis title: *Two-Dimensional Compaction Strategies*. Advisor: Prof. Robert W. Dutton.

June, 1981 *Master of Science, Electrical Engineering, Stanford Univeristy.*

June, 1980 *Bachelor of Science, Electrical Engineering, Stanford University.* Graduated with distinction.

Employment

July, 2007—present *Professor, Rhesa "Ray" S. Farmer Distinguished Chair in Embedded Computer Systems, Georgia Research Alliance Eminent Scholar, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta GA.* Teach classes in embedded computing and electrical and computer engineering. Conduct and supervise research. Courtesy appointments in the School of Computer Science, College of Management, and Bioengineering Program.

July, 1998—June, 2007 *Professor of Electrical Engineering, Princeton University, Princeton NJ.* Teach classes in embedded computing, VLSI design, computer architecture, and multimedia. Conduct and supervise research in computer-aided design of digital systems, VLSI systems, embedded computing systems, digital video architectures, and multimedia computing systems. Also Associated Faculty, Department of Computer Science.

March 2003—present *Director/Secretary/Vice President, Verificon Corporation.* Develop and license smart camera technology for surveillance and industrial applications.

October 2001—July 2002 *Chief Technical Officer, MediaWorks Technology, Schaumburg IL.* Responsible for product definition, technology development, and chip design.

July 2001—October 2001 *Chief Scientist and Principal SoC Architect, MediaWorks Technology, Schaumburg IL.* Responsible for product definition and technology development.

July, 1995—June, 1998 *Associate Professor of Electrical Engineering, Princeton University, Princeton NJ.* Taught classes in embedded system design, computer architecture, computer-aided design of digital systems, and digital video. Conducted and supervised research in computer-aided design of digital systems, VLSI systems, embedded computing systems, digital video architectures, multimedia computing systems, and digital video libraries.

September, 1989—June, 1995 *Assistant Professor of Electrical Engineering, Princeton University, Princeton NJ.* Taught classes in VLSI design, embedded system design, computer architecture, computer-aided design of digital systems, and digital video. Conducted and supervised research in embedded systems, digital video architectures and algorithms, and computer-aided design of digital systems.

September, 1988—June, 1989 *Visiting Lecturer in Computer Science, Princeton University, Princeton NJ.* Taught CS/EE 420, "Design of VLSI Systems," and CS 598C, "Advanced Topics in Computer Science: Computer-Aided Design."

August, 1984—September, 1989 *Member of Technical Staff, AT&T Bell Laboratories, Murray Hill NJ.* Conducted research in computer-aided design of digital systems: automatic layout, design representation,

register-transfer synthesis. Supervised work of co-op and summer students. Supervisors: Dr. Alfred E. Dunlop, Dr. Wolfgang Fichtner.

March, 1984—June, 1984 *Lecturer, Stanford University, Stanford CA.* Taught EE 271, "Introduction to VLSI Systems," and EE 272B, "Testing and Simulation for VLSI."

January, 1984—March, 1984 *Teaching Associate, Stanford University, Stanford CA.* Taught EE 272A, "VLSI Design Project," with Prof. Manolis Katevenis.

March 1978—March, 1984 *Research Assistant, Stanford University, Stanford CA.* Conducted research in VLSI design, maintained computer systems. Supervisor: Prof. Robert W. Dutton.

various times *Consultant.* Held consultancy or summer student positions at Silvar-Lisco, Valid, Digital Equipment Corporation, Hewlett-Packard, NEC C&C Research Lab, AT&T, Intel, Quickturn, Mentor Graphics, Advance, Inc., Clever Systems, WABTEC, Synopsys, NextSierra, Eastman Kodak.

visiting positions Visiting Professor, De Montfort University, Leicester, England (1999-2002). Visiting Professor, Stanford University (2001-2002 academic year.)

Selected Professional Activities

Vice President of Finance, IEEE Council on Electronic Design Automation, 2005-2007. General co-chair, IEEE CASES conference, 2006. Chair, ACM EMSOFT Conference, 2005. Co-Chair, IEEE MPSOC Workshop. Program co-chair, CASES conference, 2002. Board of Governors, IEEE Circuits and Systems Society, 1998-2000. Editor-in-chief, *ACM Transactions on Embedded Computing Systems*, 2001-2007. Editor-in-chief, *IEEE Transactions on VLSI Systems*, 1999-2000. Co-Editor-in-Chief, *Design Automation for Embedded Systems*, 1996-2005. General chair, ICCD '96. Workshops Chair, ACM MultiMedia '96. Technical program chair, ICCD '95. Program committee, CODES/CASHE 1996. Technical program chair, 1994 IFIP/IEEE/ACM International Workshop on Hardware-Software Co-Design (CODES). General chair, 1993 IEEE/ACM International Workshop on Hardware-Software Co-Design. Chair, Embedded Systems Track, ICCD '93. Program chair, 1992 IEEE/ACM International Workshop on Hardware-Software Co-Design. Vice Chair, Computer-Based Systems Track, IEEE ICCD '92. Program committee, ICCAD '99, '95, '94, '93, '92. Program committee, ACM International Workshop/Symposium on High-Level Synthesis 1994, 1992, 1989, 1988. Program committee, International Symposium on System Synthesis, 1995, 1996, 1998, 1999. US Vice Chair, IEEE VLSI Skills Assessment Inventory committee. Program committee, 1989 ACM/IEEE Module Generation and Silicon Compilation Workshop.

Fellow, ACM, IEEE. Member, SPIE, ASEE.

Awards

IEEE Circuits and Systems Society Education Award, 2006.

ASEE Frederick E. Terman Award, 2003.

IEEE Computer Society Golden Core Award, 2002.

Fellow, Association for Computing Machinery, 2001.

Fellow, Institute of Electrical and Electronics Engineers, 1998.

Elected to Phi Beta Kappa and Tau Beta Pi.

Dissertations and theses supervised

Mark Reichelt, *An Improved Cell Model for Hierarchical Layout Compaction*, S. M. Thesis, Massachusetts Institute of Technology, May, 1987 (with Prof. Jonathan Allen).

Andres Takach, *An Automata Model for the High-Level Specification and Synthesis of Digital Circuits and Systems*, Ph.D. dissertation, Princeton University, August, 1993.

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Chun-Yao Huang, *Joint Datapath/Controller Performance Optimization of VLSI Systems*, Ph.D. dissertation, Princeton University, August, 1994.

Ti-Yen Yen, *Hardware-Software Co-Synthesis of Distributed Embedded Systems*, Ph.D. dissertation, Princeton University, June, 1996.

Santanu Dutta, *VLSI Issues and Architectural Trade-offs in Advanced Video Signal Processors*, Ph.D. dissertation, Princeton University, July, 1996.

Michael Kozuch, *Video Service Systems for Networked Video Libraries*, Ph.D. dissertation, Princeton University, July, 1997 (with Prof. Andrew Wolfe).

Yanbing Li, *Hardware-Software Co-Synthesis of Embedded Real-Time Multiprocessors*, Ph.D. dissertation, Princeton University, August, 1998.

Hong Heather Yu, *Digital Multimedia Library Indexing and Retrieval*, Ph.D. dissertation, Princeton University, August, 1998.

Zhao Wu, *Architectural Evaluation of Multi-Cluster Wide-Issue Video Signal Processors*, Ph.D. dissertation, Princeton University, August, 1999.

David Rhodes, *Real-Analysis, ALAP-Guided Synthesis of Real-Time Embedded Systems*, Ph.D. dissertation, Princeton University, August 1999.

Jason Fritts, *Architecture and Compiler Design Issues in Programmable Media Processors*, Ph.D. dissertation, Princeton University, January 2000.

Haris Lekatsas, *Code Compression for Embedded Processors*, Ph.D. dissertation, Princeton University, August 2000.

Yuanlong Wang, *A Distributed Architecture and Crossbar Scheduling Algorithm for High Performance Switch Fabrics*, Ph.D. dissertation, Princeton University, May 2002.

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Shengqi Yang, *Low-Power System Design: Considering Reliability and Security*, Ph.D. dissertation, Princeton University, March 2006.

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Jiang Xu, *Design, Modeling, and Analysis of Networks-on-Chips for Systems-on-Chip*, Ph.D. dissertation, Princeton University, January 2007.

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EXHIBIT B

EXHIBIT B

OTHER CASES IN WHICH PROFESSOR WAYNE WOLF HAS TESTIFIED AS AN EXPERT WITNESS (PARTIAL LIST)

Mentor Graphics Corporation v. Quickturn Design Systems, Inc.
Docket Number: CV 96-342-RE
UNITED STATES DISTRICT COURT FOR THE DISTRICT OF OREGON

APTIX Corporation, META Systems, Inc. v. Quickturn Design Systems, Inc.
Case Number: C 98-00762 WHA
UNITED STATES DISTRICT COURT FOR THE NORTHERN DISTRICT OF CALIFORNIA

Mentor Graphics Corporation et al. v. Quickturn Design Systems, Inc. and Cadence Design Systems, Inc.
Case Numbers: C 00-1030 SI, 99-5464 SI, 00-3291 SI, 02-1426 SI
UNITED STATES DISTRICT COURT FOR THE NORTHERN DISTRICT OF CALIFORNIA

GE Harris Railway Electronics, L.L.C., and GE-Harris Railway Electronics Services, L.L.C. v. Westinghouse Air Brake Company.
Civil Action Number: 99-070-GMS
UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE

AGENCY TESTIMONY OFFERED BY PROFESSOR WAYNE WOLF

Agency: United States International Trade Commission
Investigation Number: 337-TA-383
Complainant: Quickturn Design Systems, Inc.