Project profile

Cluster for Application and Technology Research in Europe on NanoElectronics

CT312 | Manufacturing Solutions Targetting Competitive European Production in 3D [MASTER_3D]

PROJECT CONTRIBUTES TO

Communication	
Automotive and transport	✔
Health and ageing society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	✔
More Moore	
Technology node	130 nm

The CATRENE MASTER_3D project will contribute to the transformation of European Union leadership in the R&D of 3D integrated circuits (ICs) into 3D IC manufacturing leadership. Manufacturing methods to maximise process robustness and yield, minimise ramp-up time, support high volume production and reduce manufacturing cost will be developed and implemented in consortium members' fabs. The activities will focus on 3D ICs with through-silicon-vias (TSVs) and wafer-level-packaging (WLP). Manufacturing excellence will be addressed by tool enhancements to support high yield, mass production and the development of novel in-line metrology methods.

Partners:

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ISIS
NXP
PVA AS
QUALTERA SAS
Rockwood Wafer Reclaim SAS
SPTS Technologies SAS
STMicroelectronics

Project leader:

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Key project dates:

Start: December 2012
End: November 2015

Countries involved

Austria
Belgium
France
Germany
Israel

The MASTER_3D project aims to achieve excellence in 3D IC production by developing and implementing techniques to enable cost competitive manufacturing. Several 3D IC yield models will be developed to allow the impact of various yield detractors to be quantified.

Master 3D will provide the base-ground for the demonstration and manufacture of highly-miniaturised energy-efficient devices that make use of short, low-noise, interconnects.

In the context of this project, the work includes 3D IC which covers bonded layers of ICs interconnected with TSVs, as well as other components of 3D stacking such as stacked chips applying advanced interconnects like redistribution layer or wafer bumps as well as technology components that will be investigated in MASTER_3D, excluding standard packaging components.

Reaching the expected 3D IC standard of manufacturing excellence involves the development of manufacturing methods for competitive 3D IC production in Europe. Building on the results of other relevant projects such as JEMSIP, COCOA and ESIP, the MASTER_3D project will develop and implement 3D IC manufacturing methods for in-line and electrical parametric monitoring and built in robustness, as well as yield enhancement and testing.

Manufacturing cost reduction will also be addressed with specific focus on TSVs and WLP.

Testing in production

In order to accurately quantify the progress in manufacturing effectiveness, thanks to MASTER_3D, global objectives will be made available in terms of yield improvement and cost reduction for 3D ICs manufactured on the production lines of the silicon chip manufacturers (SCMs) in the consortium.

Each of the participating integrated design manufacturers (IDMs) plans to introduce one 3D IC to mass production during the project and will use it as a test vehicle to assess the methods developed.

The aim is to validate a >30% cost reduction target and a >30% overall yield enhancement of this test vehicle over the period of the project.

To achieve those objectives, MASTER_3D will focus on:

- Process tools assessment and improvement
- Failure analysis in the mass production environment
- Characterisation and metrology methods and tools
- Test infrastructure and strategy
- Yield modelling and improvement

From R&D lead to manufacturing lead

The CATRENE programme supports the European Community efforts to implement 3D IC manufacturing in the mobile and multimedia, micro-electro-mechanical-systems (MEMS) and sensor integration sectors and to develop and manufacture a wide range of complex systems-on-chip (SoCs).

In 2009, the TSV market was $0.299 billion and by 2015 is expected to grow to $4.719 billion. While image sensors have historically been the largest users of TSV technologies, memory packaging will be the largest market in 2015 (source IBS Sept. 2010). Europe has a strong R&D position in 3D IC development as well as in a number of other areas but it also has a perennial weakness in its ability to transform the conversion of R&D into manufacturing leadership. Far Eastern competitors such as Toshiba, already started to manufacture 3D Opto ICs in 2007 and are again about to take the lead in the manufacture of 3D ICs.

On the other hand, decisive action in implementing 3D IC integration using TSVs and WLP in EU fabs would provide a unique opportunity to regain some of the packaging part of the value chain from oriental competitors.

If we consider the value chain of 3D TSVs with respect to other assembly solutions, we can see that interface technologies cover a wider area than that of previous assembly solutions. To keep these interface technologies in Europe on the silicon foundry and IDM side is a key challenge that remains achievable because TSVs and WLP are typically produced in wafer fabs which are well-established in Europe. Additionally, 3D ICs will be the basis of a broad variety of devices and technologies, challenging the implementation of smart production schemes, which is also a European strength. Nevertheless, capturing this part of the 3D value chain will only be possible if European SC manufacturers can be competitive with respect to open source appropriate technology (OSAT) solutions.

Cost competitive manufacture

The MASTER_3D project aims to make the most of this opportunity by developing and implementing manufacturing methods to enable cost competitive manufacturing of 3D ICs in Europe. This relates particularly to the field of "Communication & Digital Lifestyles", which is likely to be the first major market for 3D ICs, followed by "Manufacturing".

However, the project has general relevance for all work areas because 3D IC integration can be applied to any semiconductor product and will also address 'green' issues due to less material usage and energy consumption through wide input-output (IO) technology for chip-to-chip communication that will be demonstrated by several partners. The MASTER_3D project will measurably support the EU effort towards "growth and jobs" in Europe by specifically strengthening the European manufacturing competitiveness for 3D integrated circuits.

3D integration of ICs is the most significant innovation in semiconductor technology for decades. It is forecast that 3D integrated ICs will have a share of 10% of the global semiconductor market already by 2015 with a double digit annual growth rate. This is largely driven by the substitution of existing systems with new 3D ICs to enable system miniaturisation, cost reduction and performance improvement.

Success has its risks

Europe has gained some R&D leadership in this field. However there is a risk that Europe will fall behind Far Eastern competitors by taking this technology to manufacturing with large negative economic effects far beyond the semiconductor industry. It is therefore necessary to put the required production environment in place that will allow Europe to play a significant role in the volume manufacture of 3D ICs. That is why the MASTER_3D project aims to transform EU leadership in R&D of 3D integrated circuits into sustainable 3D IC manufacturing leadership.

MASTER_3D will, in part, build on previous ENIAC or CATRENE R&D initiatives such as JEMSiP3D, which is developing basic tool and unit process capabilities, COCOA which is developing 3D integration concepts and ESIP which is studying 3D system-in package (SiP) reliability.

The results of this project will be disseminated widely and will confirm the excellence and competitiveness of European fabs manufacturing 3D ICs.

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

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