A 60-GHz CPW-Fed High-Gain and Broadband Integrated Horn Antenna

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***Abstract*—An integrated horn antenna is presented for 60-GHz WPAN applications. Compared with other types of antenna for 60-GHz WPAN applications, an integrated horn antenna features wide bandwidth and high gain. This integrated H-plane horn is elevated on the top of the substrate using CMOS-compatible microfabrication steps. Antenna efficiency is greatly improved after eliminating dielectric loss. This antenna is excited using an integrated vertical current probe connected with a coplanar-waveguide (CPW) by surface micromachining technologies. The lower part of the horn is constructed by rows of metallized pillars. The upper part and the top wall are built by stacking two layers of micromachined silicon wafers. The horn bottom is formed by metalizing the substrate's top surface. A prototype antenna is designed, fabricated, and characterized. Simulation and measurement results have shown wide input matching bandwidth and radiation bandwidth. The measured radiation pattern agrees well with the simulated one, demonstrating a gain as high as 14.6 dBi.**

***Index Terms*—Coplanar waveguide, integrated horn, micromachining, millimeter wave, *V*-band.**

I. Introduction

With the ever-increasing demand for low-cost and low-power wireless communication systems in the millimeter wave regime, such as 60-GHz wireless personal area network (WPAN) applications, the need for integrating all function modules (digital, RF, optical, etc.) on a single chip or into a single package becomes more pronounced [1], [2]. Antenna integration is still a challenge. This is because an antenna has the opposite substrate requirements as the rest of the integrated functions and circuits since it prefers low ϵ_r, thick substrates to suppress the substrate modes (higher efficiency), achieve a wider bandwidth, undisturbed radiation patterns, and reduced undesired coupling between the various elements in array configurations. This is not compatible with the rest of the RF components/passives that need high ϵ_r and thin materials for the sake of compactness and thermal dissipation.

An on-chip millimeter wave antenna has advantages such as integration simplicity and compactness. However, a low-gain and narrow-band millimeter-wave on-chip antenna can severely degrade the system's signal-to-noise ratio (SNR) and waste the power-saving or gain-boosting efforts from the active circuitry. In [3] and [4], an antenna gain around $-7\sim-9$ dBi was measured for a dipole antenna, far below its optimal value.

On the other hand, there are many high-performance antennas developed on antenna friendly substrates such as liquid crystal polymer (LCP) or substrates with very low loss such as low-temperature co-fired ceramic (LTCC) [5], [6]. However, integration and packaging complexity, as well as potential performance degradation from a hybrid interconnect, has hindered more progress from being made with this method.

To the best knowledge of authors, although many papers have been published for stand-alone components, only a few have reported 60-GHz antenna integration accomplishments and issues from a system point of view. Among them, [7] reported a high-efficiency antenna using a system-in-package approach. [8] reported a 2×2 array designed for transceiver integration. One common limitation of these works is that the antenna gain is not very high. An array with more elements can lead to a higher gain, but loss from feeding networks will lower the efficiency.

An integrated horn is a good candidate to overcome all of the above limitations. It was introduced in [9] and has generated extensive interest because of its high gain, high efficiency, and wide bandwidth. Several millimeter-wave and submillimeter-wave receivers that integrate mixers with horn antennas have been reported and shown to have superior performance [10]–[15], where a couple of silicon wafers are wet-etched along a certain crystal orientation and stacked to form the horn flare. In most cases, the horn axis is aligned perpendicular to the substrate surface. The number of layers needed for a good gain is still practical for THz and submillimeter wave for the broadside radiation [11], [12]. It is not feasible though for lower frequencies since a significant number of silicon wafer must be used with different opening for different layers to generate a stepped tapering profile. Integrated horns designed for end-fire radiation were also reported, as in [12] and [13]. Fewer layers are needed for this configuration. This reduces fabrication cost and is adopted in this paper.

However, another important issue with all of these designs is their relatively complicated feeding schemes. A microstrip probe, a dipole or a slot ring can be used to excite the horn [9]–[14]. However, almost all of these excitation structures need to be fabricated separately on another substrate (silicon, quartz or a thin film dielectric substrate) and inserted into an individual microstrip channel. This complicates the fabrication and assembly steps, thus increasing the fabrication cost.

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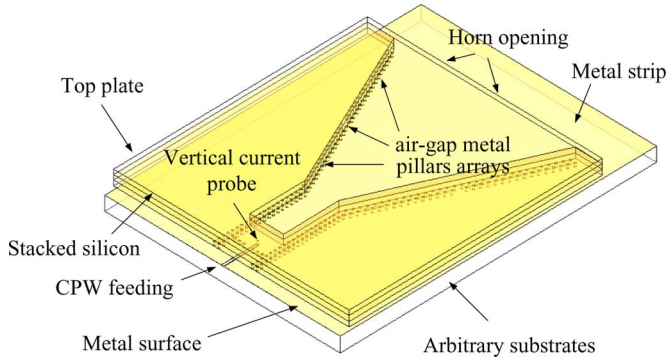

Fig. 1. 3-D view of the proposed micromachined horn.

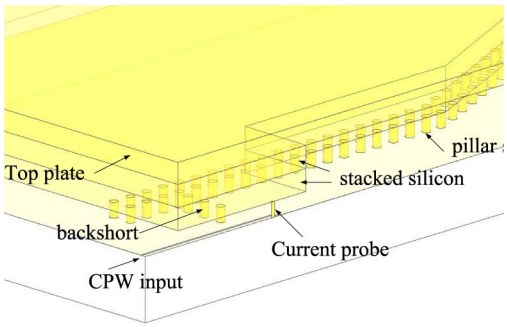

Fig. 2. The close-up schematic for the feeding structure (splitted along the symmetry plane).

In our previous research, we reported a CPW-connected vertical monopole using the SU-8 based polymer core conductor, which can be used either as a radiator or a current probe to excite other elevated millimeter-wave structures [16]–[20]. Here, it is used to excite an integrated waveguide which tapers linearly to a horn antenna. The lower part of the sidewall is constructed by rows of metalized pillars. The upper part and the top wall are built by stacking two layers of micromachined silicon wafers. The horn bottom is formed by metalizing the substrate's top surface. The horn axis is along the surface's tangential direction. Although an E-plane flare is also achievable by using multiple stepped wafers, the fabricated horn is flared only in the H-plane for simplicity.

Several advantages are claimed for the proposed horn structure, including a simple integrated feeding structure, a CMOS-compatible monolithic integration scheme, high gain, and wide bandwidth.

II. Design of the Proposed Horn Structure

A. Design of the Feeding and Transition

Fig. 1 shows the proposed horn structure. It starts from a coplanar-to-rectangular waveguide transition. After the waveguide mode is established, the waveguide tapers out in the H-plane to form the horn. A novel and simple feeding scheme for the 60 GHz horn is developed in this paper. Fig. 2 depicts the proposed feeding schemes and Fig. 3 shows the top and side view of the horn. A 350 μm-high current probe, along with 350 μm high pillar sidewalls are fabricated using SU-8 surface

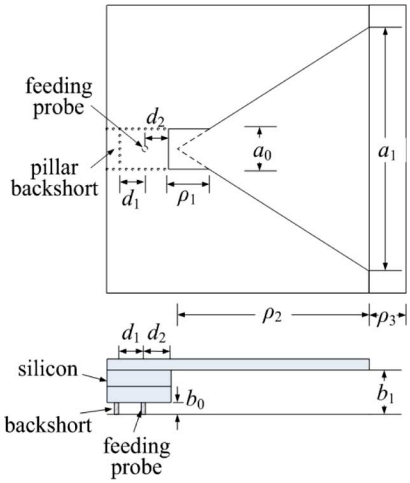

Fig. 3. Illustration of horn dimensions (top and side views).

micromachining technologies on top of the substrate. In the proposed technology, cores of pillar arrays are formed by patterning a thick, photo-definable polymer SU-8 and then plating their outer surface up to several microns. Although it is possible to directly pattern solid walls, pillar fences are used instead to satisfy processing rules, which has been discussed in [19]. The lower part of the waveguide/horn cavity is formed in this way. Two identical pieces of 525- μm-thick micromachined silicon wafers are etched through to form the upper hollow part of the horn. These two pieces have a recession for backshort different from the one formed by pillar arrays (in other words, $d_2 > 0$ in Fig. 3; otherwise, there is no contact between the probe and the silicon layer). As can be seen from the cross-section view in Figs. 2 and 3, a step profile is formed. The top plate is lowered in the transition region to contact the current probe and comes back to its regular height for the waveguide and horn to achieve a high gain operation. The length of the backshort (d_1 in Fig. 3) and the distance from the current probe to the step edge (d_2 in Fig. 3) are critical for impedance matching. Fig. 4(a) and (b) shows the impact of d_1 and d_2 on impedance matching, respectively. As can be seen, changing the length of the backshort d_1 affects both real and imaginary parts of the input impedance; varying the step length d_2 shifts the resonant frequency and the matching level.

B. Design of the Horn

After the TE_{10} mode is established, the waveguide flares out in the H-plane to increase the effective radiation aperture, resulting a narrow beamwidth in the H-plane. Flaring-out in the E-plane is also possible using more stepped silicon pieces to further increase the gain and narrow down the E-plane beam. Another possible solution to reduce the E-plane beamwidth is to use a tapering slot on the top plate [15].

A linear flare in the H-plane only is used in this paper and the dimensions of the horn are found following the guidelines provided in [21] to maximize the gain. Table I summarizes the horn's physical dimensions, while their physical meanings are shown in Fig. 3. A solid wall version is designed first to save full-wave simulation time. After the horn performance is optimized,

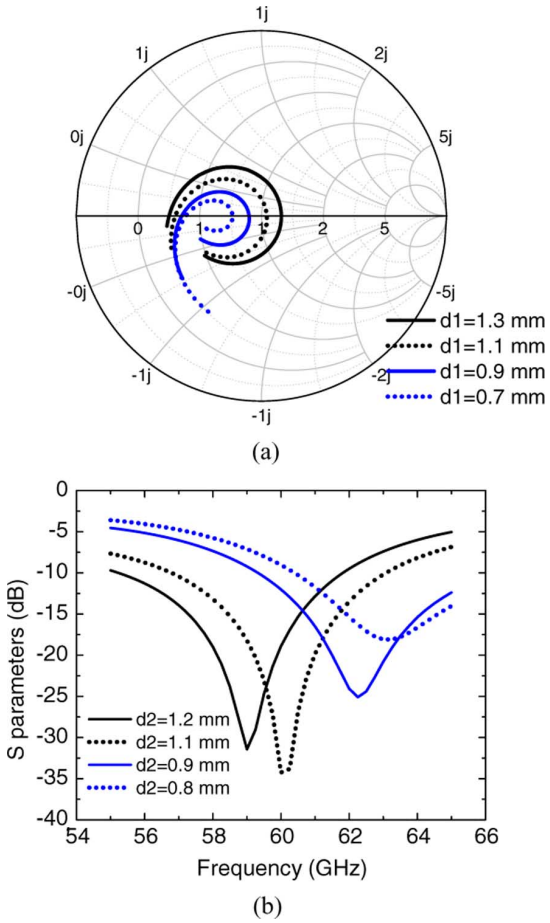

Fig. 4. (a) Input matching contours while varying d_1. (b) Reflection coefficient while varying d_2.

TABLE I
OPTIMIZED HORN DIMENSIONS WITH TRANSITION (UNITS: mm)

Dimensions	Value	Dimensions	Value	Dimensions	Value
a_0	3.7	a_1	20.0	d_1	1.0
b_0	0.35	b_1	1.4	d_2	0.9
ρ_1	6.1	ρ_2	18.0	ρ_3	6.0

the lower part of the sidewall is replaced with rows of pillars using the following equations [22]:

$$a_{\text{eff}} = a - d^2/0.95b \tag{1}$$

where a_{eff} is the width of the equivalent solid-wall waveguide that has the same characteristic impedance and a is the measured center to center distance between the two inner rows of pillars, d is the diameter of the pillar and b is the pitch between two adjacent pillars. d and b were chosen to minimize the EM-wave leakage while meeting the fabrication constrains [22]. Further adjustments are made with the aid of the full wave simulator. As shown in Fig. 5, return loss larger than 10 dB is observed to cover the unlicensed 7 GHz bandwidth at 60 GHz for WPAN applications.

The relatively narrow bandwidth, compared with the one of a conventional mechanically machined stand-alone horn, is attributed to the simple-to-fabricate feeding scheme we choose

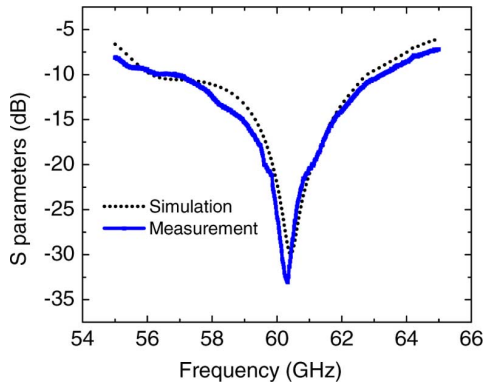

Fig. 5. Simulated and measured return loss of the proposed horn.

in this design. If the height of the waveguide is linearly tapered from the height of the pillar to the height of a standard WR-15 waveguide (1.91 mm), a larger bandwidth can be easily achieved. This linear tapering can be approximated by stacking staggered silicon pieces. The other possible scheme is to use a noncontact feeding scheme described in [17], where the whole V-band from 50 to 75 GHz can be covered. By slightly increasing the fabrication complexity for the silicon micromachined parts, the bandwidth improvement can be easily achieved but it was not pursued in this design.

A 14.6-dB gain is predicted by multiple full wave simulation tools including Ansoft HFSS and Flomerics Microstripes. This value is close to the one (15 dBi) that is required to transmit 10-mW power for a 10-m range within a channel bandwidth of 2.16 GHz in high rate physical layer, according to recommendations from WirelessHD industry consortium [23].

A further practical consideration for the horn is the opening and the sidewall can not be too close to the wafer edge. This is because radiation is easily blocked or affected by any objects close to transceiver packaging if the horn opening is at the wafer edge. Moreover, SU-8 coating has an edge bead. Pillars in this region have a large height difference with other pillars, thus a good contact with top layers can not be made.

To address the above concern, a 6-mm metal strip outside the horn opening (refer to Fig. 1) is used on top of the substrate as a margin between the outermost SU-8 pillar for the horn sidewall and the wafer edge. Simulation finds this metal strip width has the effect of tilting the main radiation beam to the upper space and boost the antenna gain by coherently reflecting outgoing waves to the upper space. It is also found that the maximal beam is pointed to $\theta = 60^\circ$ direction. To better describe the radiation beamwidth, a tilted H-plane is defined as shown in Fig. 6 since a regular H-plane is less meaningful when the radiation beam is tilted. 3-dB beamwidth on E-plane and this tilted H-plane is $44^\circ(38^\circ$–$82^\circ)$ and $20^\circ(-10^\circ$–$10^\circ)$, respectively. Beamwidth on the tilted H-plane is obviously narrower than the one on E-plane since this is a H-plane horn.

It should be noted that the beam-tilting can be avoided by also extending the top silicon cover. However, in our fabrication, we align the top cover exactly on the outermost pillars to simplify our alignment between the layers.

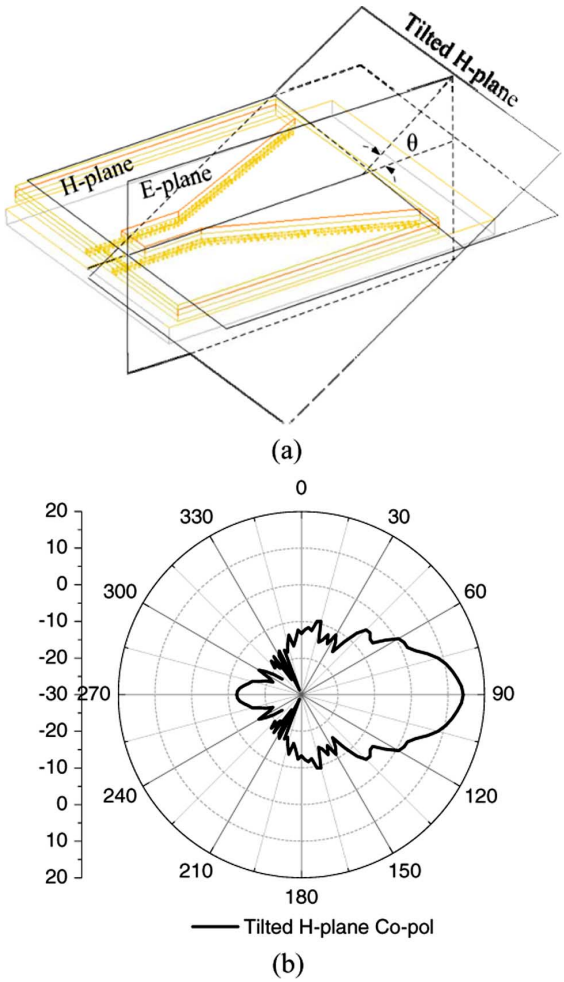

Fig. 6. Radiation pattern cut planes definition and simulated radiation pattern on tilted H-plane.

III. Fabrication and Measurement

Fabrication of pillar arrays for the lower part of horn sidewalls follows the same process flow described in [20] and is shown in Fig. 7. An SEM picture shows the pillars in Fig. 8. Fabrication of micromachined silicon pieces starts from the cleaning process. A silicon dioxide layer with 0.5-μm thickness is deposited on the silicon wafer (whose bulk resistivity is 10 000 ohms-cm) using Unaxis PECVD as a stop layer. Then, the silicon wafer is flipped over and the photoresist (PR), SRP 220 is spun on it. After the soft baking, the wafer is patterned using MA6 mask aligner and etched through using STS ICP with DRIE process until the stop layer. Once the PR remnants and the stop layer are removed, the metals, Ti/Cu/Au, with the thickness of 20 nm/3 μm/20 nm are sputtered on the silicon sample using dc sputter.

In terms of compatibility with MMIC integration, all processes involved are standard microelectronics fabrications steps. However, the best approach to use this technology is to introduce it in the post-silicon stage, after all active and passive circuits have been formed on the silicon substrate.

The assembly flow to further illustrate how this horn antenna is built is shown in Fig. 9. Alignment between different layers is achieved with the aid of an acrylic fixture. Fig. 10 shows pictures before and after the acrylic fixture cover is closed.

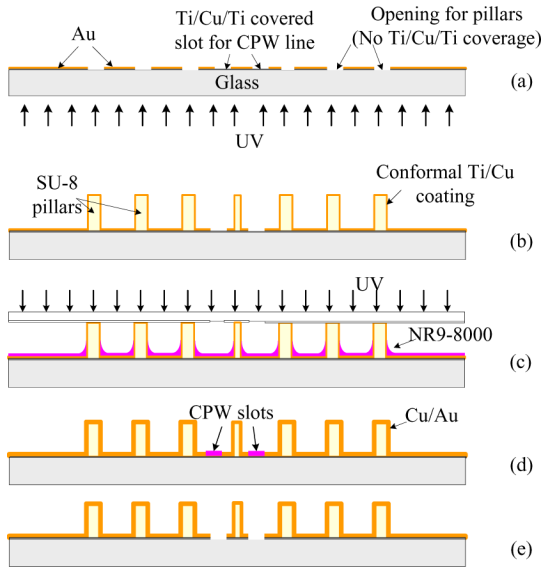

Fig. 7. Fabrication flow of polymer-core-condutor pillars.

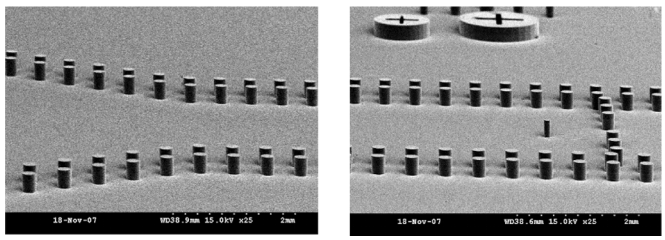

Fig. 8. SEM pictures for the micromachined horn showing the feeding probe and the horn flare pillar sidewall.

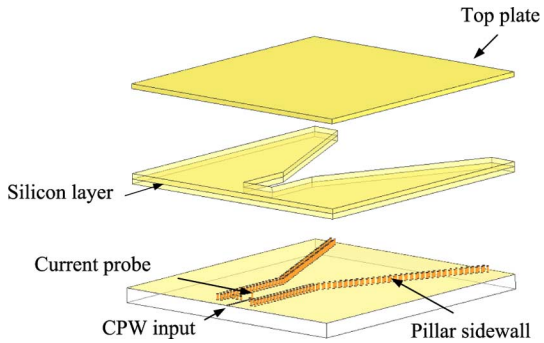

Fig. 9. The assembly scheme for the horn structure layer by layer.

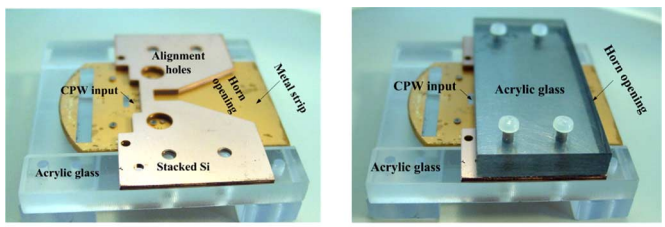

Fig. 10. Pictures of the horn antenna assembly.

The fabricated sample on a glass substrate is measured by an Agilent 8510XF vector network analyzer station connected with GSG probes of a 250-μm pitch. The system is calibrated

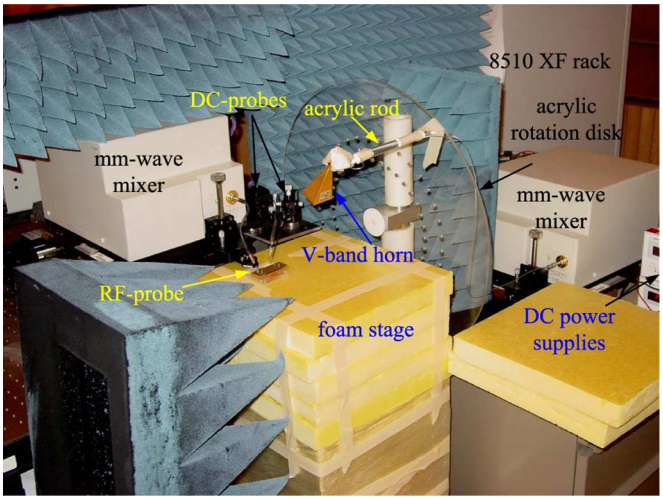

Fig. 11. On-wafer pattern measurement setup.

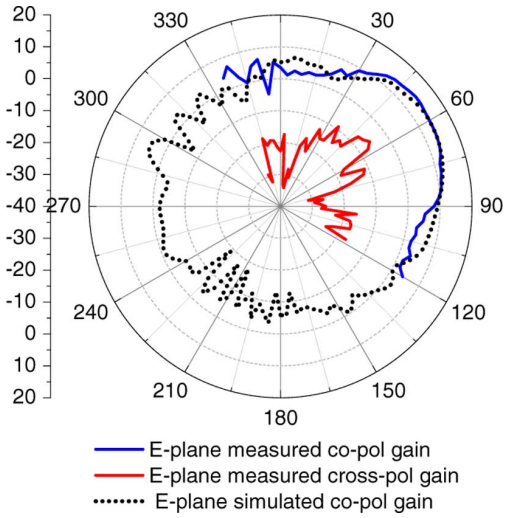

Fig. 12. Simulated and measured E-plane gain patterns.

with WinCal SOLT scheme between 55 and 65 GHz. The reference plane is set to the probe tips. The measurement results are plotted in Fig. 5 (along with the HFSS full-wave simulation result). Good agreement between simulation and measurement is observed. Larger than 10-dB return loss was observed from 56.9 to 63.2 GHz. The resonance was found at 60.3 GHz, which is slightly off the 60 GHz. The discrepancy is within fabrication tolerance. It might also be attributed to misalignment between metalized SU-8 pillars and silicon pieces. A 100-μm misalignment between pillars and silicon pieces was found. This can be corrected by using a micromachined alignment piece in the future.

Pattern measurement is taken using an on-wafer pattern measurement setup based on an Agilent 110 GHz VNA. Fig. 11 shows a picture of the on-wafer pattern measurement to characterize this antenna.

Radiation patterns are measured on both E- and H-planes at 60.3 GHz, which is the measured resonant frequency. From full-wave simulations, the gain is not sensitive in the vicinity of 60 GHz. The peak radiation was found at the same direction as predicted by the simulations. To measure the peak gain value, the system is calibrated with two identical WR-15 25-dBi gain horns; the standard-gain horn antenna is connected to Port 1 of the network analyzer and pointed to the peak direction that is already known. Then the received power is compared at Port 2 with the one measured from the fabricated horn. The gain can be calculated after considering all connector losses, including 2-dB insertion loss from the Cascade probe and 1.2-dB insertion loss from the WR-15 to coaxial adapter.

The measured E-plane copolarization gain pattern, E-plane cross-polarization gain pattern, and the simulated E-plane co-polarization gain pattern, are plotted together in Fig. 12. Discrepancies between simulations and measurements can be found in Fig. 12, especially in the angular regions where the radiation is weak. This is attributed to a limited dynamic range of measuring radiation patterns using a PNA for the purpose of on-wafer probing. Other factors include reflections from test setups that cannot be avoided even though the best efforts have been attempted to minimize the reflections.

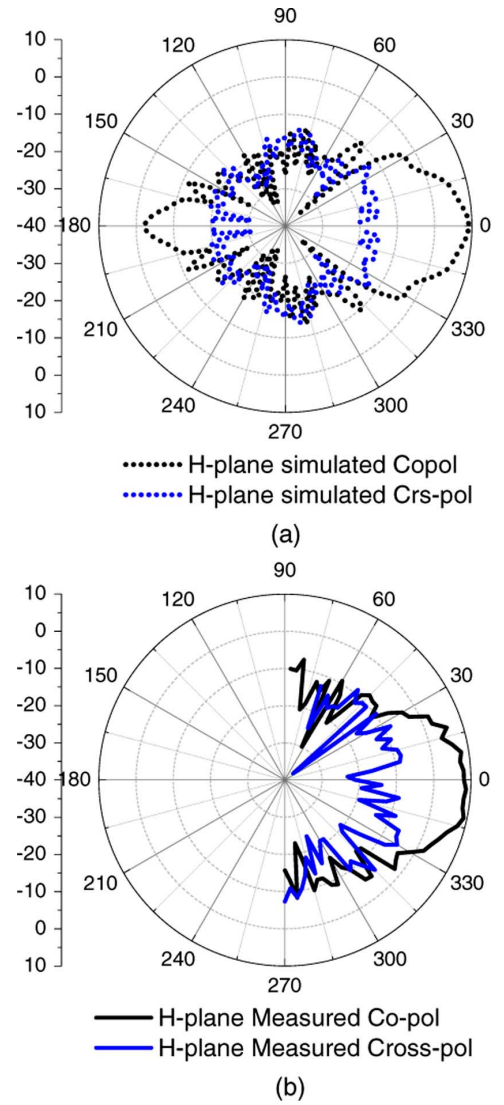

Fig. 13. (a) Simulated and (b) measured H-plane gain patterns.

Simulated and measured H-plane gain patterns are separately plotted in Fig. 13(a) and (b) for clarity. Since the main radiation beam is tilted to the upper space, H-plane radiation patterns are

less informative than the E-plane pattern. Still, agreement between simulation and measurement is great and a narrower beam width can be observed on the H-plane.

IV. Discussion and Conclusion

An integrated horn antenna is presented in this paper. By combining thick-film surface micromachining and silicon bulk micromachining technologies, a CPW-fed air-filled horn antenna is developed and characterized for 60-GHz applications. A wide bandwidth and a measured high gain of 14.4 dBi is observed in simulations and measurements. The combination of these two brings the possibility to lower the integration cost and maintain the system performance at the same time.

The 60-GHz Wireless HDTV and other millimeter-wave radio technologies, such as 77-GHz auto radar, are targeting low-cost high-volume consumer electronics applications. A high performance, millimeter-wave passive component is no longer a luxury just for military and defense applications. However, for most wireless HDTV prototypes demonstrated, millimeter-wave antennas have to be integrated on/into prohibitively expensive military-grade microwave materials, it is good for prototyping but not good for massive production.

On the contrary, our proposed method to implement millimeter wave antennas will have huge advantages when it is going to massive production stage. It does not require a low-loss substrate, thus reducing cost on materials. It relies on the standard photolithography technology, a thick-film epoxy and the standard metalization technologies. It is easier to be integrated with MMICs than the traditional waveguide-based horn antennas [24]. Using micromachined silicon pieces to get the upper part of the horn antenna is just one example and other low-cost materials can also be used to demonstrate the advantages we have claimed.

In general, the proposed method offers an easy integration platform of both planar components and 3-D integrated modules on top of the substrate.

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References

[1] R. R. Tummala *et al.*, "The SOP for miniaturized, mixed-signal computing, communication and consumer systems of the next decade," *IEEE Trans. Adv. Packag.*, vol. 27, no. 2, pp. 250–267, May 2004.

[2] M. M. Tentzeris *et al.*, "RF SoP for multi-band RF and millimeter-wave systems," *Adv. Packag. Mag.*, pp. 15–16, Apr. 2004.

[3] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, and I. Seto, "A 60-GHz CMOS receiver front-end with frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1030–1037, Apr. 2008.

[4] M. Sanduleanu and J. Long, "CMOS integrated transceivers for 60 GHz UWB communication," in *Proc. IEEE Int. Conf. Ultra-Wideband (ICUWB 2007)*, Sep. 24–26, 2007, pp. 508–513.

[5] J. Lee, N. Kidera, S. Pinel, J. Laskar, and M. M. Tentzeris, "Fully integrated passive front-end solutions for a v-band ltcc wireless system," *IEEE Antennas Wireless Propag. Lett.*, vol. 6, pp. 285–288, 2007.

[6] I. K. Kim, N. Kidera, S. Pinel, J. Papapolymerou, J. Laskar, J.-G. Yook, and M. M. Tentzeris, "Linear tapered cavity-backed slot antenna for millimeter-wave LTCC modules," *IEEE Antennas Wireless Propag. Lett.*, vol. 5, pp. 175–178, Dec. 2006.

[7] T. Zwick, D. Liu, and B. Gaucher, "Broadband planar superstrate antenna for integrated millimeterwave transceivers," *IEEE Trans. Antennas Propag.*, vol. 54, no. 10, pp. 2790–2796, Oct. 2006.

[8] S. Sarkar and J. Laskar, "A single-chip 25pj/bit multi-gigabit 60 ghz receiver module," in *Proc. IEEE/MTT-S Int. Microw. Symp.*, Jun. 3–8, 2007, pp. 475–478.

[9] G. Eleftheriades, W. Ali-Ahmad, L. Katehi, and G. M. Rebeiz, "Millimeter-wave integrated-horn antennas. I. Theory," *IEEE Trans. Antennas Propag.*, vol. 39, no. 11, pp. 1575–1581, Nov. 1991.

[10] T. Budka, M. Trippe, S. Weinreb, and G. M. Rebeiz, "A 75 GHz to 115 GHz quasi-optical amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 5, pp. 899–901, May 1994.

[11] K. Hui, J. Hesler, D. Kurtz, W. Bishop, and T. Crowe, "A micromachined 585 GHz Schottky mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 10, no. 9, pp. 374–376, Sep.. 2000.

[12] J. Hesler, K. Hui, R. Dahlstrom, R. Weikle, T. Crowe, C. Mann, and H. Wallace, "Analysis of an octagonal micromachined horn antenna for submillimeter-wave applications," *IEEE Trans. Antennas Propag.*, vol. 49, no. 6, pp. 997–1001, Jun. 2001.

[13] B. Shenouda, L. Pearson, and J. Harriss, "Etched-silicon micromachined W-band waveguides and horn antennas," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 4, pp. 724–727, Apr. 2001.

[14] V. Douvalis, H. Yang, and C. Parini, "A monolithic active conical horn antenna array for millimeter and submillimeter wave applications," *IEEE Trans. Antennas Propag.*, vol. 54, no. 5, pp. 1393–1398, May 2006.

[15] J. Digby, C. McIntosh, G. Parkhurst, B. Towlson, S. Hadjiloucas, J. Bowen, J. Chamberlain, R. Pollard, R. Miles, D. Steenson, L. Karatzas, N. Cronin, and S. Davies, "Fabrication and characterization of micromachined rectangular waveguide components for use at millimeter-wave and terahertz frequencies," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 8, pp. 1293–1302, Aug. 2000.

[16] B. Pan, Y. Yoon, P. Kirby, J. Papapolymerou, M. M. Tentzeris, and M. Allen, "A W-band surface micromachined monopole for low-cost wireless communication systems," in *Proc. IEEE-IMS Symp.*, Fort Worth, TX, Jun. 2004, pp. 1935–1938.

[17] Y. Li, B. Pan, M. M. Tentzeris, and J. Papapolymerou, "A fully micromachined W-band coplanar waveguide to rectangular waveguide transition," in *Proc. IEEE-IMS Symp.*, Honolulu, HI, Jun. 2007, pp. 1031–1034.

[18] Y.-K. Yoon, J.-W. Park, and M. G. Allen, "Polymer-core conductor approaches for RF MEMS," *J. Microelectromech. Syst.*, vol. 14, no. 5, pp. 886–894, Oct. 2005.

[19] B. Pan, Y. Li, M. M. Tentzeris, and J. Papapolymerou, "A high-Q millimeter-wave air-lifted cavity resonator on lossy substrates," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 8, pp. 571–573, Aug. 2007.

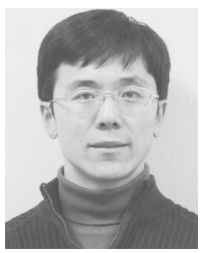
[20] B. Pan, Y. Li, M. M. Tentzeris, and J. Papapolymerou, "High performance surface micromachined millimeter-wave cavity filters," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 4, pp. 959–970, Apr. 2008.

[21] C. Balanis, *Antenna Theory*, 2nd ed. New York: Wiley, p. 678.

[22] D. Deslandes and K. Wu, "Accurate modeling, wave mechanisms, and design considerations of substrate integrated waveguide," *IEEE Trans. Microw. Theory Tech.*, vol. 54, pp. 2516–2526, Jun. 2006.

[23] , [Online]. Available: http://www.wirelesshd.org/

[24] B. Pan, Y. Li, G. E. Ponchak, M. M. Tentzeris, and J. Papapolymerou, "A low-loss substrate-independent approach for 60 GHz transceiver front-end integration using micromachining technologies," *IEEE Trans. Microw. Theory Tech.*, Dec. 2008.



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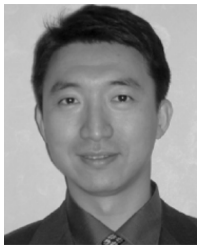

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