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Dale Becker received the B.E.E degree from the University of Minnesota, M.S.E.E. from Syracuse University and the Ph.D. from the University of Illinois at Urbana Champaign. He is a Chief Engineer of Electronic Packaging Integration in IBM Systems and a member of the IBM Academy of Technology. His responsibility is the electrical system architecture of IBM Systems including the design of high-speed channels to enable the computer system performance and the power distribution networks for reliable operation of the integrated circuits that make up the processor subsystem.

Dr. Becker has chaired the IEEE EPEPS Conference in 2010, 2014, and 2016 and has co-chaired the 2014 IEEE EMCS embedded conference on SIPI TPC as well as 2017 EMCS Global University Chair. He has been a distinguished lecturer in the EMC Society. He has patents on electrical design of computer systems and has presented papers in refereed journals and international conferences covering many aspects of electrical computer system design including power distribution analysis and design and modeling of signal and power distribution networks. He is an IEEE Fellow, an iNEMI Technical Committee member, and a member of SWE.

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From 1989 to 1996 Mr. Cheng worked for the Sun Microsystems Corporation, Ca. USA, as a Signal Integrity engineer. From 1996 to 1999, he worked for Intel Corporation, CA, USA, as a Principal Engineer. In July 1999, he joined 3PAR Data Corporation as a Principal Engineer, Fremont, CA. Currently he is with Storage Division in Hewlett-Packard Enterprise Company as a Distinguished Technologist.

Paul D. Franzone is currently a Distinguished Professor of Electrical and Computer Engineering and Director of Graduate programs in ECE at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Adelaide, Australia. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom and three companies he cofounded, Communica, LightSpin Technologies and Polymer Braille Inc. His current interests center on the application of, technology and design of complex microsystems incorporating VLSI, advanced packaging and nano-electronics. He has lead several major efforts

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An-Yu Kuo is currently Sr. Group Director of the Sigrity R&D Group of Cadence Design Solutions. He is responsible for development of SI/PI/EMI/RF simulation tools. After working for two engineering consulting companies, Dr. Kuo founded Optimal Corporation in 1995 to develop simulation software for package designs. Optimal was acquired by Apache Design Solution in 2007. As a Chief Architect at Apache, Dr. Kuo helped integrating IC and package/board thermal simulation tools into a single tool. In 2009, Dr. Kuo joined Sigrity as a director to develop 3D full-wave EM tool, 3DFEM, and electrical/thermal co-simulation function inside PowerDC. Dr. Kuo joined Cadence after Cadence acquired Sigrity in 2012

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Tim Michalka has spent thirty years working in signal and power integrity, primarily on the electrical aspects of electronic packaging and interconnections, including tenures at Digital Equipment Corporation, the Hewlett-Packard Company, and currently Qualcomm Technologies Incorporated where he is a Sr. Director of Engineering managing the Power and Signal Integrity Group. His team works with engineers across the company to deliver leading edge wireless communications integrated circuits by applying electromagnetic and circuit level simulation tools in conjunction with high frequency electrical measurements. He received a BS degree in Electrical Engineering from the University of Maine in 1982 and MS and PhD degrees in Electrical Engineering from Stanford University in 1983 and 1988 respectively.



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Elyse Rosenbaum is the Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. She received the B.S. degree (with distinction) from Cornell University in 1984, the M.S. degree from Stanford University in 1985, and the Ph.D. degree from the University of California, Berkeley in 1992, all in electrical engineering. From 1984 through 1987, she was a Member of Technical Staff at AT&T Bell Laboratories in Holmdel, NJ.

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Madhavan Swaminathan is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE) and Director of the Center for Co-Design of Chip, Package, System (C3PS), Georgia Tech. He formerly held the position of Joseph M. Pettit Professor in Electronics in ECE and Deputy Director of the NSF Microsystems Packaging Research Center, Georgia Tech. Prior to joining Georgia Tech, he was with IBM working on packaging for supercomputers. He is the author of 450+ refereed technical publications, holds 29 patents, is primary author and co-editor of 3 books, and was founder and co-founder of two start-up companies (E-System Design and Jacket Micro Devices) and founder of the IEEE Conference Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the CPMT society on Signal Integrity in the Asian Region. He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE EMC society. He received his M.S. and Ph.D. degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.