electronics

MDPI

Article

A Modular Power Converter Topology to Interface Removable Batteries with 400 V and 800 V Electric Powertrains †

Duberney Murillo-Yarce *, Gabriel D. Colvero, Alexis A. Gómez, Jairo Tuñón Díaz, Alberto Rodríguez and Aitor Vázquez

Electrical, Electronics, Comunications and Systems Engineering Department, University of Oviedo, 33204 Gijón, Spain; dacanalgabriel@uniovi.es (G.D.C.); gomezalexis@uniovi.es (A.A.G.); tunonjairo@uniovi.es (J.T.D.); rodriguezalberto@uniovi.es (A.R.); vazquezaitor@uniovi.es (A.V.)

* Correspondence: murilloduberney@uniovi.es

† This paper is extended version of Proceedings of the Energy Conversión Congress and Expo (ECCE Europe 24'), Darmstadt, Germany, 2–6 September 2024 and Proceedings of the 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 25–29 February 2024.

Abstract: Electric vehicles (EVs) are a sustainable means of transportation, with their on-board batteries being crucial for both performance and energy management. A modular and reconfigurable power converter topology to connect removable batteries to the main DC bus of an EV is proposed in this paper. By employing Dual Active Bridge (DAB) converters in an Input Parallel Output Series (IPOS) configuration, the proposed topology is compatible with 400 V and 800 V standards without the need for external switches. The research explored the possibility to apply a very simple control strategy based on independent linear regulators. A theoretical analysis of the IPOS DAB converter is presented and the design of independent control regulators which minimize the coupling effect between the control variables is addressed. The stability of the IPOS DAB converter could be ensured using the proposed simplistic approach, enabling us to drastically simplify the regulator design step. The dynamic performance of the system was confirmed by means of a simulation and experimentally.

Keywords: DC-DC converter; dual active bridge; electrical vehicles; reconfigurable topology; removable battery

Academic Editors: Jingyang Fang, Heshou Wang, Hongjian Lin, Dong Xie, Yuanxi Chen and Xiangyu Meng

Received: 29 November 2024
Revised: 20 December 2024
Accepted: 3 January 2025
Published: 7 January 2025

Citation: Murillo-Yarce, D.; Colvero, G.D.; Gómez, A.A.; Díaz, J.T.; Rodríguez, A.; Vázquez, A. A Modular Power Converter Topology to Interface Removable Batteries with 400 V and 800 V Electric Powertrains. *Electronics* **2025**, *14*, 215. https://doi.org/10.3390/electronics14020215

1. Introduction

Electric vehicles (EVs) are now one major point of interest for power electronics, due to the need for environmentally sustainable transportation methods and for the greater implication of power electronics in EVs in comparison with internal combustion vehicles [1,2]. The single heaviest element comprising the powertrain of an EV is the high-voltage (HV) battery. In most current commercial EVs, there is only one battery; therefore, the performance and range of the EV are conditioned and limited by its technology and capacity. To optimize the capacity and weight of the battery of an EV, modular battery arrangements have been studied [3].

A simplified example of a multiple battery powertrain is illustrated in Figure 1. In this example, there is a main battery and two smaller removable batteries. Each battery possesses a Battery Management System (BMS) that monitors different parameters related to the State of Charge (SoC) and overall health of the battery packs. A separate Battery Unit Management System (BUMS) reads the information of all BMS units and controls the DC-DC converters that interface the removable batteries with the main DC bus. The main battery is the primary power source.

Several advantages can be attributed to such an architecture. The range and performance of the EV can be adjusted in a dynamic manner according to the expected use of the vehicle by removing or adding more batteries. This approach allows for the combination of different battery voltages and technologies. Then, it is possible to maximize their respective strengths and to mitigate their weaknesses. Moreover, this opens the possibility to adopt second-life batteries as a removable energy storage system in EVs or vice versa [4].

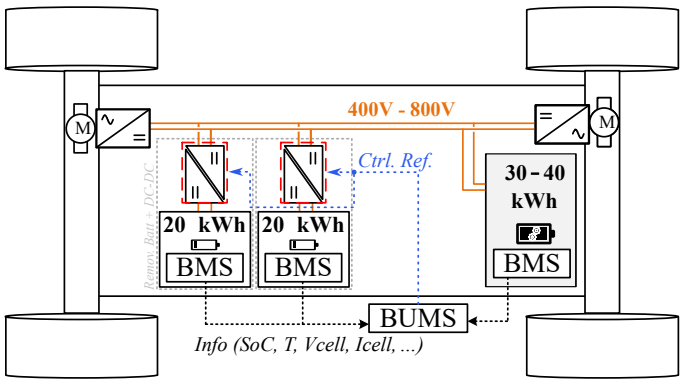


Figure 1. EV power system with multiple batteries.

The removable batteries are connected to the main DC bus through a DC-DC converter, as depicted in Figure 1. Currently, commercial EVs commonly use two voltage standards for the DC bus: 400 V and 800 V. While the 400 V standard dominates today, the shift to 800 V is anticipated due to its advantages, such as reduced copper requirements in conductors [5]. Ideally, the converter would be able to connect the battery to both voltage standards, while maintaining high performance across two significantly different high-side voltage ranges.

In [6], a DAB converter with two independent outputs was used. The outputs were connected in series for the 800 V DC bus or in parallel for the 400 V DC bus. The same was proposed using a resonant converter in [7]. In [8], the gain of the converter was doubled by splitting the output DC bus by changing the HV-side connections of the converter. In all these cases, external switches were necessary to connect, in different manners, the HV ports or components of the converters. These external switches increase the complexity of the topology and may reduce its performance. In [9], a modified resonant converter achieved a wide voltage operating range by combining phase shift and switching frequency modulations. And in [10], a resonant converter alternated between full-bridge and half-bridge configurations to halve the voltage gain as required. These types of control strategies are slightly more complex than traditional modulations.

A modular converter topology based on the DAB converter was proposed in [11,12], capable of operating with 400 V and 800 V DC bus standards without the need for external switches. In this paper, a small-signal average model for this modular topology was derived, identifying a coupling between the control variables of the different modules. Control loops were developed to regulate different state variables, ignoring the control variable coupling. A dynamic simulation and experimental tests were used to ensure the stability and performance of the system. The structure of this paper is as follows. In Section 2, the proposed topology for each individual module and the complete topology are detailed, providing small-signal average models for both. In Section 3, the controller's design is outlined. In Section 4, the experimental and simulation verification of the dynamic performance of control loops is provided. Finally, conclusions are detailed in Section 5.

2. Proposed Topology

As mentioned in the Introduction, this paper proposes the use of a modular topology. To further clarify this, the proposed topology that corresponds to the different DC-DC converters depicted in Figure 1 and that are associated with the removable batteries is in reality composed of multiple independent converters connected to each other, and each individual converter is a module of the complete topology. Contrary to the solutions presented in [6–8], the physical connections of the different modules are always the same; therefore, there is no need for external switches, and only the operation mode of the individual modules is changed when connected to the different DC bus standard. In contrast with [9], with a wide voltage range, the individual converters may be designed for a more reduced operating range, further optimizing their performance.

2.1. Fundamental Module

Galvanic isolation was adopted as a requirement at the individual module level. This improves the flexibility of the overall topology and opens up a wider voltage range for the removable batteries that could be lower than the DC bus voltage. Furthermore, this approach fits with potential future safety regulations for removable batteries in EVs. The module must operate with good performance in a relatively small range of input and output voltages. It must also provide good current regulation capabilities to face sudden changes in the operating power due to vehicle demands.

Taking into account these requirements, a suitable topology is the Dual Active Bridge (DAB), which is a very well-known topology in the field of EVs and power electronics in general [13,14]. The structure of the DAB converter is shown in Figure 2.

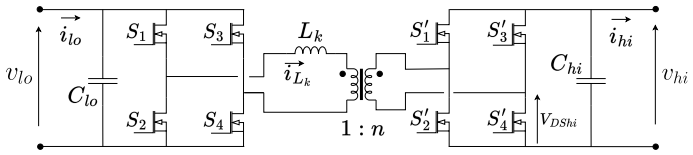


Figure 2. Structure of the DAB converter.

S_1 to S_4 are the low-voltage-side switches, v_{lo} is the low-voltage-side voltage, i_{lo} is the low-voltage-side current, C_{lo} is the low-voltage side capacitor, L_k is the leakage inductor and i_{L_k} its current, S'_1 to S'_4 are the high-voltage-side switches, C_{hi} is the high-voltage-side capacitor and i_{hi} and v_{hi} are the current and voltage of the high-voltage-side port.

One of the simplest controls for a DAB is the Single Phase Shift (SPS) modulation. It consists of phase-shifting the bridges while both bridges operate with a duty cycle of 0.5. In this paper, no other modulation was considered. The reason for this was that this modulation offers considerable input and output voltage ranges while maintaining good efficiency and simplicity. If a greater range were necessary, more complex modulations could be used, such as a Dual Phase Shift [15] or Triple Phase Shift [16]. The average input and output currents of the DAB when operating with an SPS can be obtained from the steady-state analysis conducted in [14]:

$$\langle i_{lo} \rangle_T = \frac{(1-d)dT\langle v_{hi} \rangle_T}{nL_k}, \tag{1}$$

$$\langle i_{hi} \rangle_T = \frac{(1-d)dT\langle v_{lo} \rangle_T}{nL_k}, \tag{2}$$

where T is half the switching period and d is the normalized phase shift between the primary and secondary bridges. Under normal operation, the input and output voltages may be considered constant during a switching period.

In [14], an average model for the DAB when using an SPS was derived. The model was obtained using the Current Injected Equivalent Circuit Approach (CIECA) [17]. The basic idea of this method is to replace the converter with a quadrupole made up of two non-linear dependent current sources. These current sources must behave in the same manner as the average converter currents that they replace (see Figure 3). Thus, the value of the current source that corresponds to the low-voltage (LV) port coincides with (1), whereas the value of the current source for the HV port coincides with (2).

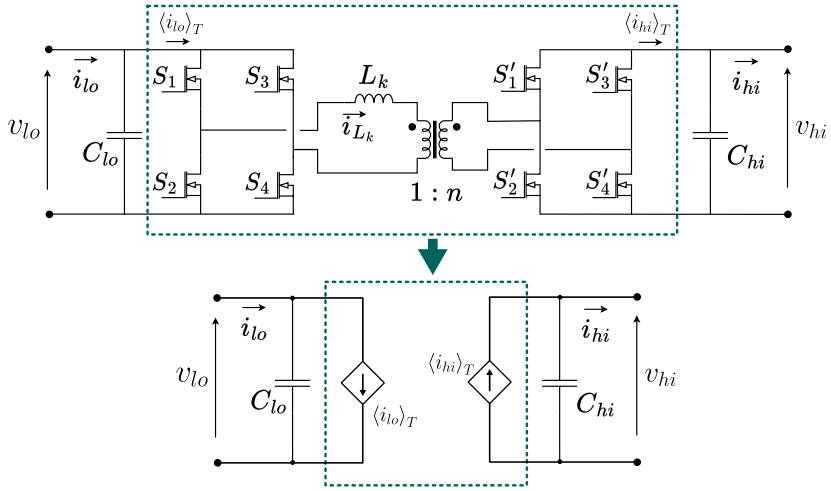


Figure 3. Descriptive CIECA schematic.

It is important to note that the derived large-signal model exhibits a sampling delay inherent to the averaging process. This delay will only be noticeable when trying to visualize phenomena close to the switching frequency of the converter and, therefore, this effect may be neglected when utilizing classical linear control theory. The average model is non-linear, and it is not possible to derive classical transfer functions directly. By applying small perturbations around an operating point to the average model variables, the small-signal canonical circuit depicted in Figure 4 is obtained.

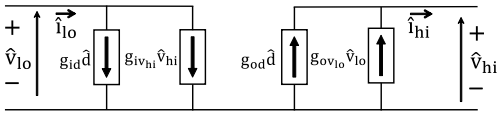


Figure 4. Small−signal average canonical circuit of the DAB converter.

By observing the circuit, the input and output current perturbations can easily be obtained:

$$\hat{i_{hi}} = \left|\frac{\partial i_{hi}}{\partial d}\right|_o \hat{d} + \left|\frac{\partial i_{hi}}{\partial v_{lo}}\right|_o \hat{v}_{lo} = g_{od}\hat{d} + g_{ov_{ol}}\hat{v}_{lo}, \tag{3}$$

$$\hat{i_{lo}} = \left|\frac{\partial i_{lo}}{\partial d}\right|_o \hat{d} + \left|\frac{\partial i_{lo}}{\partial v_{hi}}\right|_o \hat{v}_{hi} = g_{id}\hat{d} + g_{iv_{hi}}\hat{v}_{hi}, \tag{4}$$

where

$$g_{od} = \frac{(1-2D)TV_{lo}}{nL_k}, \tag{5}$$

$$g_{ov_{lo}} = \frac{(1-D)DT}{nL_k}, \tag{6}$$

$$g_{id} = \frac{(1-2D)TV_{hi}}{nL_k}, \tag{7}$$

$$g_{iv_{hi}} = \frac{(1-D)DT}{nL_k}. \tag{8}$$

The variables in capital letters correspond to the operating point, whereas the ones with a circumflex accent (hat) correspond to the small-signal perturbations. Additionally, second-order effects were considered negligible for the small-signal analysis. These equations show that the input and output currents present no dynamics and that an instant change in the phase shift, input voltage or output voltage means an instant change in the input or output currents. In reality, these changes can be considered effective in the next switching cycle.

2.2. Configurations

As mentioned in the Introduction, various modular topologies address the challenge of operating in two distinct output voltage ranges through different configurations. The most straightforward modular arrangements to tackle the issue of different DC bus voltage standards, one being the double of the other, are the Input Parallel Output Parallel (IPOP) configuration for the 400 V standard and the Input Parallel Output Series (IPOS) configuration for the 800 V standard. This approach is usually based on two or more identical converters that connect their output ports by means of external switches. Although modular arrangements can be made with several modules, in this paper, only two modules were considered.

Strictly speaking, the proposed topology uses the same configuration regardless of the DC bus voltage standard. All modules are always physically connected in an IPOS configuration. For the 400 V standard, all modules operate in series at the output and several modules may be turned off. To achieve this off state, all switches on the HV side are turned on simultaneously while all the LV switches remain off. In the case of the 800 V standard, the same connections remain and all modules operate in series at the output and divide the bus voltage between their respective HV ports. Both cases are depicted in Figure 5a,b. The set of both DAB converters or individual modules constitute the DC-DC topology that interfaces the removable batteries with the DC bus, marked in red in Figure 1.

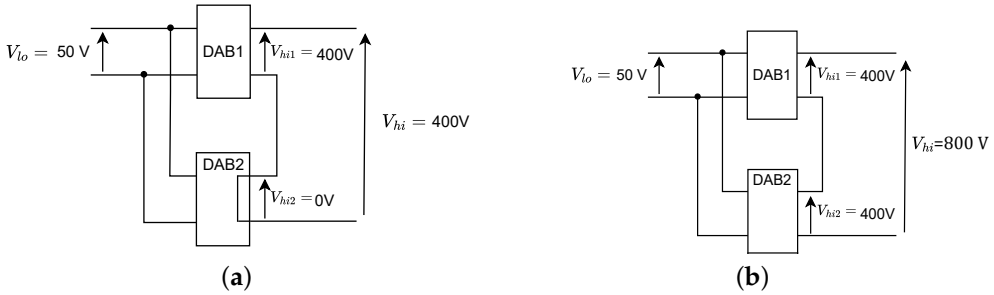


Figure 5. Modular topologies and configurations for standard bus DC voltages: (**a**) 400 V standard, (**b**) 800 V standard.

The BUMS (see Figure 1) collects and monitors the voltage and current data of individual batteries, including the main battery. The high-voltage-side voltage of one module is directly measured, while the output voltage of the other module is determined as the difference between this value and the HV DC bus voltage, which is derived from the output voltage of the main battery. In the case of currents, a single sensor is used to control the power transfer by the system, as depicted in Figure 6. Note that the current sensor is placed at the input port. The BUMS will provide the converter with the appropriate current reference based on the aforementioned data and the powertrain control strategy.

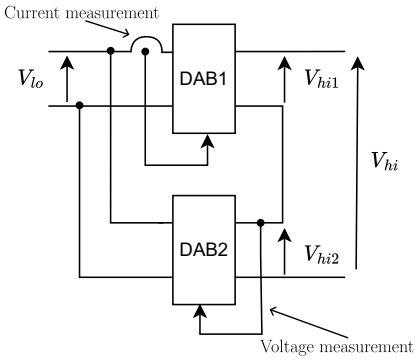


Figure 6. IPOS test setup.

3. Controller Design for the Reconfigurable Topology

Considering the small-signal average canonical circuit depicted in Figure 4 and the IPOS configuration used for the HV DC bus standard, a drawing of the resulting small-signal average circuit is shown in Figure 7. In this schematic, the input capacitor of each of the converters was not drawn as they all are connected directly with an ideal voltage source. Additionally, the converters are represented with a unique current source on the HV side and two on the LV side; this is because the input voltage of the converters was considered constant and no small-signal perturbations were considered.

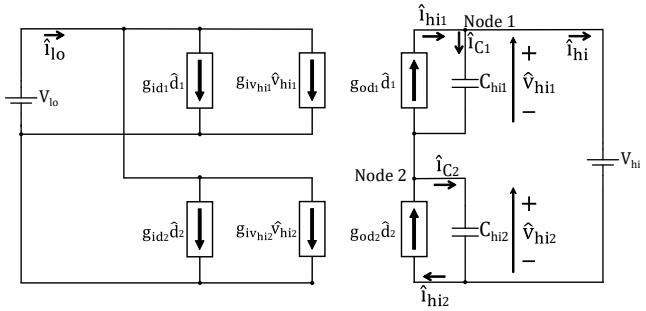


Figure 7. Small−signal average canonical circuit for IPOS connection.

Using Kirchhoff's current law on nodes 1 and 2, the result is

$$\hat{i_{hi_j}} = \hat{i_{hi}} + \hat{i_{C_j}}, \tag{9}$$

where $\hat{i_{C_j}}$ is the current increment for the high voltage side capacitor of the respective converter. By definition, the increment in the voltage of a capacitor is given by

$$\hat{v_{hi_j}} = \frac{\hat{i_{C_j}}}{C_j s}, \tag{10}$$

and by combining (3), (9) and (10), the resulting HV port voltage increment equation for each module is

$$\hat{v_{hi_j}} = \frac{g_{od_j}\hat{d}_j - \hat{i_{hi}}}{C_j s}. \tag{11}$$

Notice that in (11), the control to output transfer function g_{od} was referenced with the subindex j. This is to account for the possibility of different module designs. As the global high-voltage-side voltage is fixed by the DC bus, the sum of the high-voltage-side voltage perturbations must be null:

$$\sum_j \hat{v_{hi_j}} = 0. \tag{12}$$

By adding (11) for both HV module ports and considering that all modules are identical and operate under the same conditions, an expression for the output current increment is derived:

$$\hat{i_{hi}} = \frac{g_{od}}{2}\left(\hat{d_1} + \hat{d_2}\right), \tag{13}$$

and an expression for the output voltage perturbation of the modules can be derived by combining (13) with (11):

$$\hat{v_{hi_1}} = \frac{g_{od}}{2Cs}\left(\hat{d_1} - \hat{d_2}\right) = -v_{hi_2}. \tag{14}$$

As the controlled variables are v_{hi_1} and i_{lo_2}, (13) can be related to i_{lo_2} with

$$\hat{i_{lo2}} = \frac{\hat{i_{hi_2}} V_{hi_2}}{V_{lo_2}} + \frac{I_{hi_2}\hat{v_{hi_2}}}{V_{lo_2}}. \tag{15}$$

Finally, these equations can be put into a matrix form:

$$\begin{bmatrix} \hat{v_{hi_1}} \\ \hat{i_{lo_2}} \end{bmatrix} = \begin{bmatrix} A & -A \\ B[E+1] & B[E-1] \end{bmatrix} \begin{bmatrix} \hat{d_1} \\ \hat{d_2} \end{bmatrix}, \tag{16}$$

where

$$A = \frac{g_{od}}{Cs}, \tag{17}$$

$$B = \frac{g_{od}}{2V_{lo}^2(1-D)DTnL_kCs}, \tag{18}$$

$$E = \frac{V_{hi_2}nL_kCs}{V_{lo}(1-D)DT}, \tag{19}$$

and $\hat{i_{lo_2}}$ corresponds to the DAB_2 low-voltage-side current increment, V_{hi_2} is the DAB_2 operating point high-voltage-side voltage and V_{lo} is the operating point low-voltage-side voltage.

It is evident from (16) that coupling exists between the phase shift values of the different modules. To address this, equal converter parameters were assumed for all modules in deriving expressions from (11). The difference among the parameters in the DAB modules may introduce additional terms in the coupling between the control variables, as was demonstrated in [18]. However, as was established before, this parameter variation among modules was neglected in this study.

In this paper, an independent regulator design is proposed. The main goal was to obtain the simplest approach to guarantee the stable operation of the ISOP DAB converter. Hence, the solution provided here was based on designing a current loop and a voltage loop for a single DAB module, independently. Two constraints were added to the designs to minimize the coupling variable effect: an overdamped transient response and a limited bandwidth. With this approach, it was possible to apply both regulators to the ISOP DAB converter and to guarantee stable operation. This approach aimed to simplify the controller stage characteristics and to explore the limitations of the linear and independent regulators.

In a literature review on decoupling approaches, there were two overall control architectures: decentralized and centralized controls. Decentralized control approaches effectively enable the decoupling of control loops while maintaining independent control over individual modules, as demonstrated in [19–23]. In contrast, centralized control architectures can mitigate coupling effects but offer more limited modular functionality [18,24–27]. Regarding control strategies with the ability to mitigate coupling effects, these can be categorized into two main groups: linear and non-linear controls. Linear control approaches predominantly rely on PID-based structures [18,24,26] and droop control methods [22,23]. On the other hand,

non-linear control strategies include techniques such as input impedance shaping [22,25] and sliding mode control [27].

Several of the aforementioned control strategies have been applied to mitigate coupling effects between input and output ports in modular topologies, with three notable cases: (i) linear controls implemented with decoupling matrices [18,24,26], (ii) high-order impedance shaping [25] and (iii) hierarchical sliding mode control [27]. Among these decoupled control strategies, only [26,27] have been specifically applied to IPOS configurations. A linear control strategy derived its control strategy from the small-signal model in [26]. Conversely, a sliding mode approach was employed in [27], where a sliding surface was designed to drive the system toward this surface and maintain it there.

4. Simulation and Experimental Verification

The simulation results obtained in PSIM and the experimental results obtained from a power-scaled-down prototype are presented below. The reconfigurable topology consists of two DAB units (DAB_1 and DAB_2), each rated at 500 W, and these are shown in Figure 8. These DABs exhibit slight construction differences in their magnetic elements (the leakage inductance (L_k) and the transformer turns ratio (n)). In DAB_1, L_k is integrated within the transformer itself, while in DAB_2, L_k is an external inductor connected in series to the transformer (see Table 1).

Table 1. Main parameters of the DABs.

Parameter	DAB_1	DAB_2
L_k [µH]	6.2	3.3
C_{lo} [µF]	50	60
C_{hi} [µF]	3	3
n	8	8.4

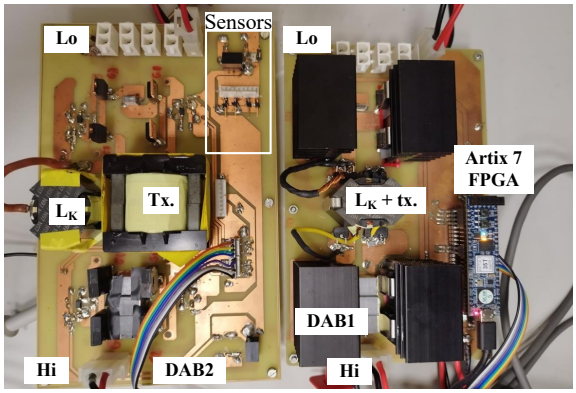


Figure 8. DAB_1 and DAB_2 prototypes. *Lo* represents the low-voltage side and *Hi* the high-voltage side. *Tx* is the transformer, and L_k is the leakage inductance (external for DAB_1 and integrated into *tx* in DAB_2).

The controller was implemented on the Artix 7 Cmod A7-35T FPGA, Digilent, Pullman, WA, USA, operating at a fixed switching frequency of 100 kHz, and it is shown in Figure 8. Initial simulations and experimental tests were conducted using a single DAB converter with integrated voltage and current sensors to independently verify the performance of the voltage and current control loops. In the final testing stage, the IPOS configuration was validated. All the experimental waveforms were obtained using an oscilloscope DSO-X-3034T model with the software version 04.08.201607 1801 from Keysight, Santa Rosa, CA, USA.

As mentioned in the previous section, this paper proposes using current and voltage control loops calculated individually for the respective modules. Figure 9 presents a generic block diagram of the voltage loop for the DAB converter, where the portion of the control loop implemented in the FPGA is shaded. The corresponding control loop for the current follows the same structure. The control loop includes a controller (H_{PWM}), compensator $(C(z))$, feedback sensor (H_{sens}), analog-to-digital converter (H_{ADC}), and DAB converter plant $(G(s))$. The gains and parameters corresponding to the voltage and current control loops are shown in Table 2. Notice that the only difference is related to the sensor gain, as different sensors are used to measure the current and voltage. The purpose of the compensator is to obtain damped responses for the loops and adjust their dynamics (faster for the current loop and slower for the voltage loop). Both the current and voltage compensators were first designed in the continuous domain, using SISOtool, as I and PI, respectively. Several design criteria were tested both theoretically and in a simulation to check for unmodeled behavior during the IPOS configuration due to control variable coupling. The selected criteria were that the voltage loop dynamics were set one order of magnitude slower than the current counterpart and the resulting compensators offered phase and gain margins of 87° and 25.8 dB for the current compensator and 73° and 57.5 dB for the voltage compensator. These were then discretized.

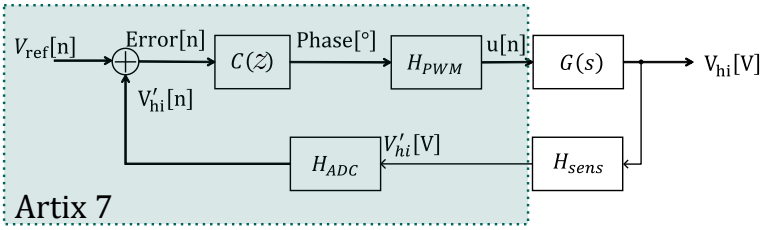


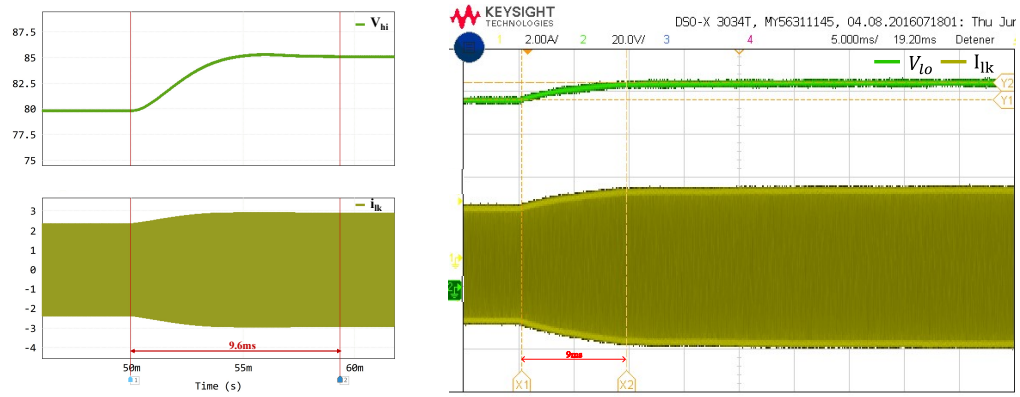
Figure 9. Voltage block diagram of the control loop implementation.

Table 2. Main parameters of the voltage and current loops.

Parameter	Voltage Loop	Current Loop
H_{PWM}	373.7	373.7
H_{ADC}	9.7×10^{-4}	9.7×10^{-4}
H_{sens}	5.2×10^{-3}	0.4
ADC Resolution (bits)	12	12
PWM Resolution (bits)	10	10

4.1. Voltage Loop

To validate the voltage loop ($C(z) = 12 + 0.12/(1 - z^{-1})$), a 5 V reference HV-side voltage step change was applied. Figure 10a,b show the simulated and experimental responses for both the HV-side voltage and the inductor current. The HV port of DAB_2 was monitored using an HCPL-7520 sensor, Broadcom, San Jose, CA, USA. The reference voltage step was introduced via the Virtual Input/Output (VIO) environment in the Vivado software, v2024.1.2. In this test, a resistor was connected to the HV side of the converter. The simulation and experimental results show a good correlation. Both results exhibited similar transient response and settling times, with 9.6 ms in the simulation and 9 ms experimentally. It can be seen that this increase in the voltage reference also produced a slight increase in the current in the leakage inductance. The transition between operating points occurred without oscillations and in a damped manner.

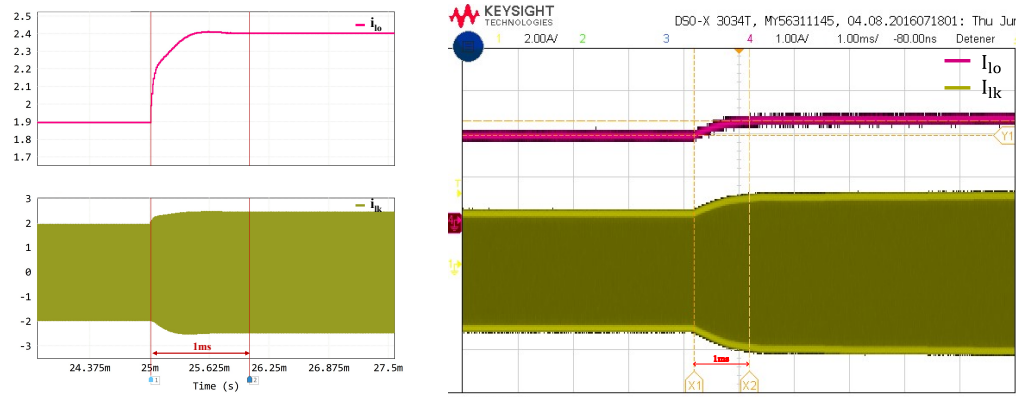


(**a**) (**b**)

Figure 10. Voltage loop response: (**a**) simulated, (**b**) experimental. CH1: i_{L_k} (2 A/div); CH2: V_{hi} (20 V/div).

4.2. Current Loop

In the same manner as the voltage loop, the current loop ($C(z) = 0.6/(1 - z^{-1})$) was verified with a step in the DAB_1 LV reference current of 0.5 A. The simulation and experimental waveforms of the LV side and the inductor current are shown in Figure 11a and Figure 11b, respectively. The current sensor used was the ACS711-25. In both the results, a damped transition was achieved between the two operating points, with a settling time of 1 ms. This settling time is consistent with the chosen compensator design criteria as the transient regime was approximately 10 times shorter than in Figure 10. During this test, two power supplies clamped the input and output voltages of the converter to 10 V and 80 V, respectively.

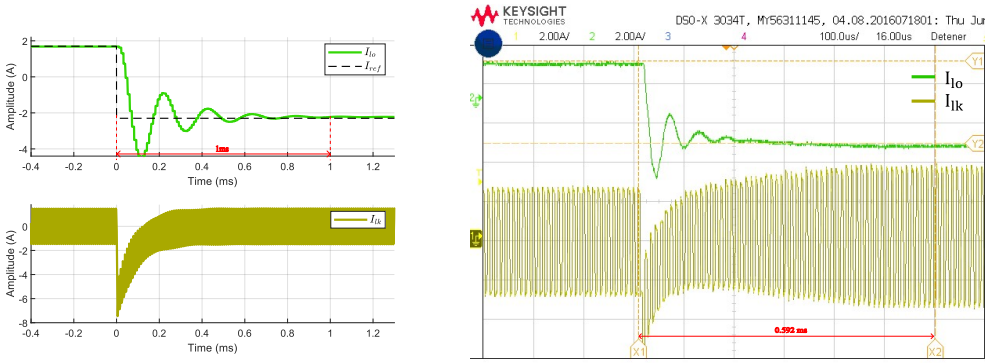


(**a**) (**b**)

Figure 11. Current loop response: (**a**) simulated, (**b**) experimental. CH1: i_{L_k} (2 A/div); CH4: i_{lo} (1 A/div).

In the voltage and current loop responses shown previously, a power transfer occurred from the LV side to the HV side ($V_{lo} \rightarrow V_{hi}$). To confirm that the current loop was capable of regulating the current in both directions, an LV-side current step with a change in the current direction from $V_{lo} \rightarrow V_{hi}$ to $V_{lo} \leftarrow V_{hi}$ was performed. The results of this step are shown in Figure 12. The dynamic behavior observed in practice was equivalent to that obtained in the simulation. In the simulation results (see Figure 12a), the sign of the current indicated the direction of power transfer. A positive current implied a power transfer from V_{lo} to V_{hi}, while a negative current meant a power transfer from V_{hi} to V_{lo}. In the experimental results shown in Figure 12b, the current i_{lo} was initially at 1.875 A. After a damped response, the current reached a final value of -2.313 A. This indicates

that the converter initially transferred 1.875 A in the V_{lo} to V_{hi} direction and then reversed, transferring 2.313 A in the V_{hi} to V_{lo} direction. The transition occurred with an overshoot of less than 2 A, and a steady state was achieved approximately 600 µs after the change. The oscillations in the LV-side current were due to the parasitic inductance of the wires used to connect the prototypes to the power supply and its dynamic response.



(**a**) (**b**)

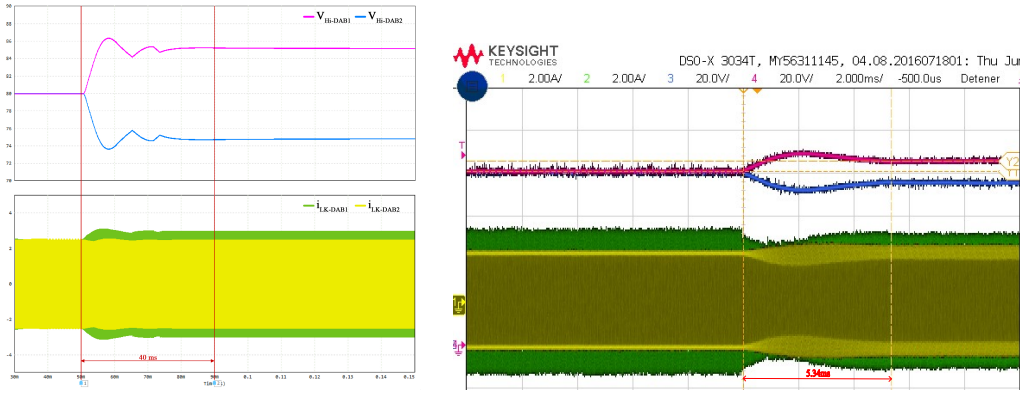
Figure 12. Result of an instantaneous change in the direction of power transfer: (**a**) simulated, (**b**) experimental. CH1: i_{L_k} (2 A/div); CH2: i_{lo} (2 A/div).

4.3. IPOS Configuration

After independently validating the voltage and current loops, simulations and experimental tests were performed with both loops in a system that included two DABs in the IPOS configuration (see Figure 6). In all cases, the LV- and HV-side voltages of the entire topology were clamped with external power supplies.

Firstly, the IPOS configuration was tested with DAB_2 turned off; this case corresponded with the 400 V standard. As this case was equivalent to a single converter, the dynamic and static responses were coincident with those already verified in Figures 10 and 11. The rest of the simulation and experimental results corresponded to the case in which both modules were active.

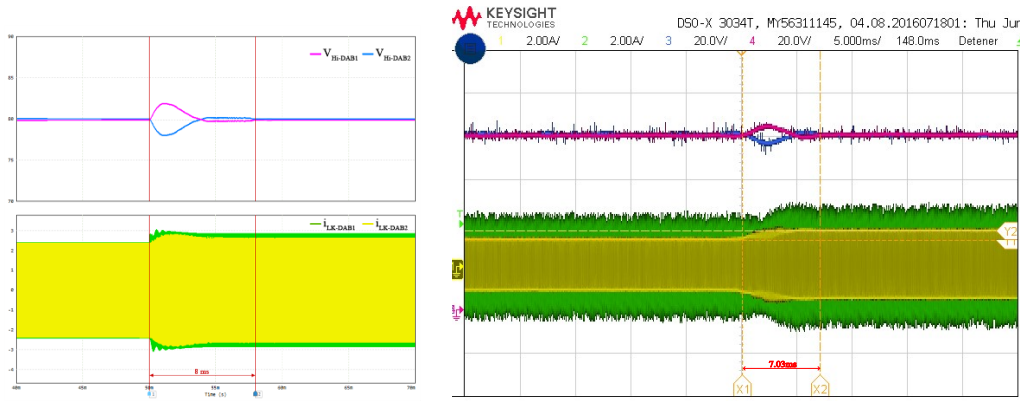
Figure 13 shows the response of the two DABs in the IPOS configuration to a change in the voltage reference of the DAB_2 HV port when transferring power from the LV side to the HV side. Figure 13a presents simulated waveforms, while Figure 13b shows the corresponding experimental results. Before the change in reference, both converters operated with a low-side voltage of 10 V and a high-side voltage of 80 V. The total series connection voltage was 160 V. Then, the reference voltage of DAB_2 was decreased by 5 V (the new reference was 75 V). The final voltage values of DAB_1 and DAB_2 were 85 V and 75 V, respectively. The current reference for the DAB_1 LV port was maintained as constant at 1.875 A. Figure 13 also shows that the change in the voltage reference produced changes in the current of the leakage inductance. This was produced by a change in the slopes of i_{lk} and the control variable coupling between control variables, as calculated in (13) and (14). Although voltage references will rarely change during operation, this test ensures adequate voltage regulation capabilities.



(**a**) (**b**)

Figure 13. IPOS connection results for the voltage loop in the V_{lo} to V_{hi} direction: (**a**) simulated, (**b**) experimental. CH1: $i_{L_k-DAB_2}$ (2 A/div); CH2: $i_{L_k-DAB_1}$ (2 A/div); CH3: V_{hi-DAB_2} (20 V/div); CH4: V_{hi-DAB_1} (20 V/div).

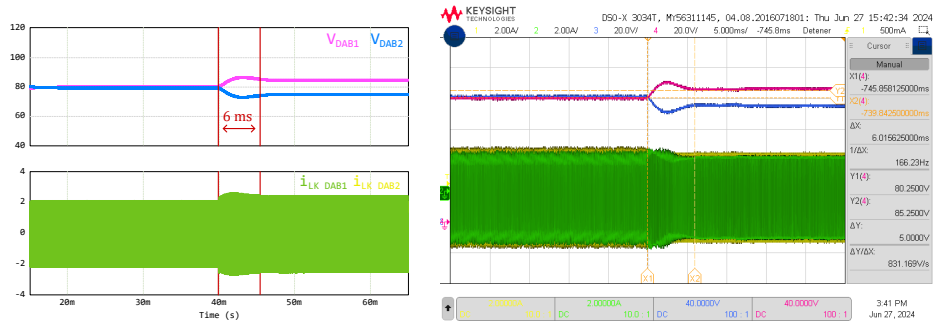
Figure 14 shows the system response to a small increase, from 1.875 A to 2.313 A, in the DAB_1 LV port current reference. The HV-side voltage reference for both converters was set to 80 V. An increase in this current while maintaining the HV-side voltage at the same level means an increase in i_{hi}. As this current is coincident for both modules in a steady state (see Figure 6), a step in the reference such as this influences the currents and operating point of both converters if the HV-side voltage distribution remains the same. Simulated waveforms are shown in Figure 14a, and the experimental results in Figure 14b. It can be noticed that the system quickly achieved steady-state currents; however, the voltage oscillations took slightly longer to return to the previous steady-state values of 80 V in each converter. This loop exhibited a faster dynamic response compared to the voltage loop.



(**a**) (**b**)

Figure 14. IPOS connection results for the current loop in the V_{lo} to V_{hi} direction: (**a**) simulated, (**b**) experimental. CH1: $i_{L_k-DAB_2}$ (2 A/div); CH2: $i_{L_k-DAB_1}$ (2 A/div); CH3: V_{hi-DAB_2} (20 V/div); CH4: V_{hi-DAB_1} (20 V/div).

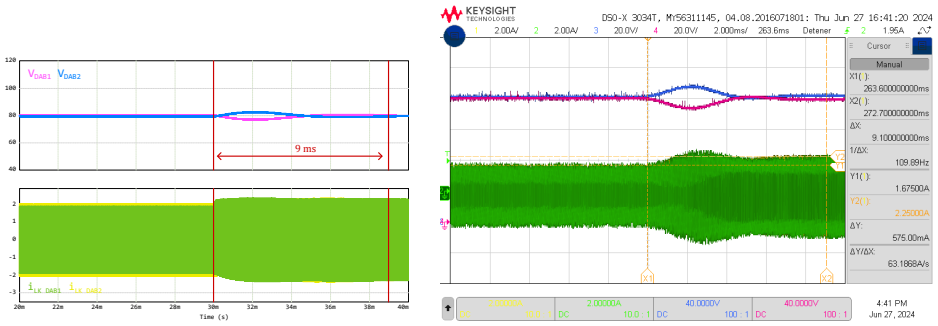
In the two previous experimental tests for the IPOS configuration, the power flowed from the LV side to the HV side. The same tests were then conducted with a reverse power direction. In Figure 15, the simulation and experimental waveforms of a reference voltage step in the HV port of DAB_2 are depicted when transferring power in the opposite direction (HV side to LV side). The step had a magnitude of -5 V, starting from 80 V. The resulting reference voltages after the step for both DABs were 85 V and 75 V for DAB_1 and DAB_2, respectively. The DAB_1 LV port current reference was set to -1.875 A. A good correlation can be observed between the simulation and experimental waveforms, as well as a similar performance to that shown in Figure 13.



(**a**) (**b**)

Figure 15. IPOS connection results for the voltage loop in the V_{hi} to V_{lo} direction: (**a**) simulated, (**b**) experimental. CH1: $i_{L_k-DAB_2}$ (2 A/div); CH2: $i_{L_k-DAB_1}$ (2 A/div); CH3: V_{hi-DAB_2} (20 V/div); CH4: V_{hi-DAB_1} (20 V/div).

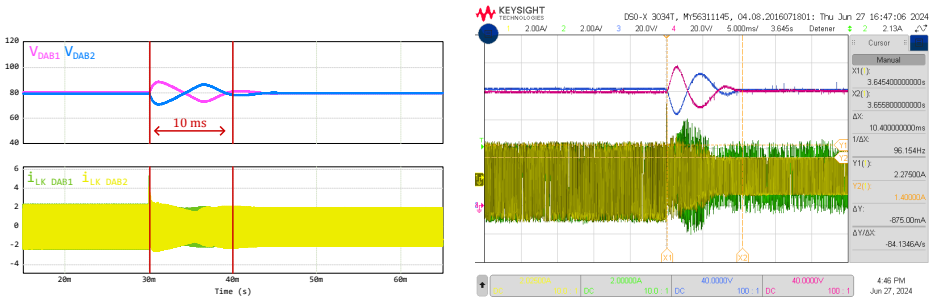
A step performed in the LV-side reference current of DAB_1 is shown in Figure 16. The original current reference was -1.875 A, and the step was -0.438 A, resulting in a final reference current of -2.313 A. The negative sign of the current indicates that power was being transferred from the HV side to the LV side. The HV reference voltages for both modules were set to 80 V. A good correlation was observed between the simulation and experimental results, and a steady state was reached rapidly. The same mutual influence as in Figure 14 was observed.



(**a**) (**b**)

Figure 16. IPOS connection results for the current loop in the V_{hi} to V_{lo} direction: (**a**) simulated, (**b**) experimental. CH1: $i_{L_k-DAB_2}$ (2 A/div); CH2: $i_{L_k-DAB_1}$ (2 A/div); CH3: V_{hi-DAB_2} (20 V/div); CH4: V_{hi-DAB_1} (20 V/div).

Finally, a test in which the flow of power was reversed while in the IPOS configuration was performed. Simulation and experimental waveforms are depicted in Figure 17. To perform this test, despite the fact that only a change in the current was performed, we had to use both control loops. Otherwise, when DAB_1 started demanding power from the HV side, its HV-side voltage might have decreased and reached an unstable operating point where the loop tried to demand more power, further reducing the voltage. If the voltage loop correctly regulates the voltage distribution on the HV side, then this scenario is avoided. The reference voltage for both converters on their HV port was set to 80 V. The DAB_1 LV-side current was set to a reference of 2.313 A, meaning a power transfer from the LV side to the HV side, and then changed to -1.875 A, thus reversing the power flow. The transient regime of this transition was relatively short, and only small voltage oscillations were observed.



(**a**) (**b**)

Figure 17. IPOS connection results for reverse power direction step: (**a**) simulated, (**b**) experimental. CH1: $i_{L_k-DAB_2}$ (2 A/div); CH2: $i_{L_k-DAB_1}$ (2 A/div); CH3: V_{hi-DAB_2} (20 V/div); CH4: V_{hi-DAB_1} (20 V/div).

In all tests, the control loops proved to be stable and offer adequate dynamics, especially considering the intended application of an EV.

5. Conclusions

In this article, an IPOS DAB-based modular topology without the need for external switches was proposed for connecting removable batteries to a DC bus. The dynamic model of this topology was studied for a two-module converter. This theoretical analysis demonstrated the existence of a coupling effect between the control variables in the ISOP structure. Due to this coupling, instabilities may happen if the controller stage is not carefully designed.

Two additional design constraints must be applied to use the independent control loops in the ISOP DAB converter. First, an overdamped response must be imposed on the transient response. Second, the dynamic responses must be set one order of magnitude apart between the current loop and the voltage loop.

The proposal was validated using simulation and experimental results. It was proved that it is possible to ensure the stability of the ISOP DAB converter following this approach. The obtained results show a reasonable transient response under different tests. The settling times measured were between 7 and 10 ms in a 10 V to 160 V test (80 V for each DAB) for a 2 A current reference. Positive and negative current reference steps were tested (i.e., forwarding power from the low-voltage side to the high-voltage side and vice versa) with similar results. Additionally, the two independent controllers were also tested in a positive-to-negative reference test. In that scenario, the settling time was 10 ms (similarly to the previous tests), but an overshoot in the voltage response was observed.

The previously mentioned results show a low influence of the coupling effect when the independent controllers are designed with the aforementioned constraints. However, further investigations need to be conducted in regard to this coupling effect and the limitation it poses to the independent compensator design, especially for a larger number of modules.

Author Contributions: Conceptualization, A.V. and A.R.; investigation, D.M.-Y., A.A.G. and J.T.D.; methodology, D.M.-Y., A.V. and A.R.; project administration, A.V. and A.R.; software, G.D.C. and J.T.D.; supervision, A.V. and A.R.; validation, D.M.-Y., G.D.C. and J.T.D.; writing—original draft, A.A.G. and D.M.-Y. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Spanish government under the research project MCINN-22-TED2021-130939B-I00. This work was also supported by the Principado de Asturias government through the grant “Severo Ochoa” BP21-114.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

BMS	Battery Management System
BUMS	Battery Unit Management System
DAB	Dual Active Bridge
EVs	Electrical Vehicles
IPOP	Input Parallel Output Parallel
IPOS	Input Parallel Output Series
ISOP	Input Series Output Parallel
ISOS	Input Series Output Series
SPS	Single Phase Shift
HV	High-Voltage
LV	Low-Voltage

References

1. Blaabjerg, F.; Wang, H.; Vernica, I.; Liu, B.; Davari, P. Reliability of Power Electronic Systems for EV/HEV Applications. *Proc. IEEE* **2021**, *109*, 1060–1076. [CrossRef]
2. Hou, R.; Magne, P.; Bilgin, B.; Emadi, A. A topological evaluation of isolated DC/DC converters for Auxiliary Power Modules in Electrified Vehicle applications. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 5–19 March 2015; pp. 1360–1366. [CrossRef]
3. Jangir, P.; Sangwan, V.; Kumar, R.; Rathore, A.K. Optimal Power Management of Multiple Battery Units by Power Converter System in Electric Vehicle. In Proceedings of the 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 18–21 December 2018; pp. 1–6. [CrossRef]
4. Rey, S.O.; Romero, J.A.; Romero, L.T.; Martínez, À.F.; Roger, X.S.; Qamar, M.A.; Domínguez-García, J.L.; Gevorkov, L. Powering the Future: A Comprehensive Review of Battery Energy Storage Systems. *Energies* **2023**, *16*, 6344. [CrossRef]
5. Jung, C. Power Up with 800-V Systems: The benefits of upgrading voltage power for battery-electric passenger vehicles. *IEEE Electrif. Mag.* **2017**, *5*, 53–58. [CrossRef]
6. Serban, E.; Pondiche, C.; Ordonez, M. Analysis and Design of Bidirectional Parallel-Series DAB-Based Converter. *IEEE Trans. Power Electron.* **2023**, *38*, 10370–10382. [CrossRef]
7. Aarninkhof, B.O.; Lyu, D.; Soeiro, T.B.; Bauer, P. A Reconfigurable Two-stage 11kW DC-DC Resonant Converter for EV Charging with a 150–1000 V Output Voltage Range. *IEEE Trans. Transp. Electrif.* **2023**, *10*, 509–522. [CrossRef]
8. Karneddi, H.; Ronanki, D. Reconfigurable Battery Charger With a Wide Voltage Range for Universal Electric Vehicle Charging Applications. *IEEE Trans. Power Electron.* **2023**, *38*, 10606–10610. [CrossRef]
9. Shakib, S.M.S.I.; Mekhilef, S. A Frequency Adaptive Phase Shift Modulation Control Based LLC Series Resonant Converter for Wide Input Voltage Applications. *IEEE Trans. Power Electron.* **2017**, *32*, 8360–8370. [CrossRef]
10. Sha, D.; Yang, X. Wide Voltage Input Full Bridge(FB)/Half Bridge(HB) Morphing-Based LLC DC–DC Converter Using Numerical Optimal Trajectory Control. *IEEE Trans. Ind. Electron.* **2023**, *70*, 3697–3707. [CrossRef]
11. Dacanal Colvero, G.; Murillo Yarce, D.; Tuñón Díaz, J.; Rodríguez Alonso, A.; Vázquez Ardura, A. Closed Loop Modular Topology to Interface Removable Batteries in an Electric Powertrain with 400 V and 800 V Compatibility. In Proceedings of the Energy Conversión Congress and Expo (ECCE Europe 24'), Darmstadt, Germany, 2–6 September 2024.
12. Murillo-Yarce, D.; Colvero, G.D.; Lamar, D.G.; Rodriguez, A.; Vazquez, A. A Reconfigurable Topology for Integration of Removable Batteries in an Electric Powertrain with 400 V and 800 V Compatibility. In Proceedings of the 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 25–29 February 2024; pp. 3092–3099, ISSN 2470-6647. [CrossRef]
13. Tian, J.; Wang, F.; Zhuo, F.; Cui, X.; Yang, D. An Optimal Primary-Side Duty Modulation Scheme With Minimum Peak-to-Peak Current Stress for DAB-Based EV Applications. *IEEE Trans. Ind. Electron.* **2023**, *70*, 6798–6808. [CrossRef]
14. Rodríguez, A.; Vázquez, A.; Lamar, D.G.; Hernando, M.M.; Sebastián, J. Different Purpose Design Strategies and Techniques to Improve the Performance of a Dual Active Bridge With Phase-Shift Control. *IEEE Trans. Power Electron.* **2015**, *30*, 790–804. [CrossRef]
15. Bal, S.; Yelaverthi, D.B.; Rathore, A.K.; Srinivasan, D. Improved Modulation Strategy Using Dual Phase Shift Modulation for Active Commutated Current-Fed Dual Active Bridge. *IEEE Trans. Power Electron.* **2018**, *33*, 7359–7375. [CrossRef]
16. Calderon, C.; Barrado, A.; Rodriguez, A.; Alou, P.; Lazaro, A.; Fernandez, C.; Zumel, P. General Analysis of Switching Modes in a Dual Active Bridge with Triple Phase Shift Modulation. *Energies* **2018**, *11*, 2419. [CrossRef]

17. Chetty, P. Current Injected Equivalent Circuit Approach to Modeling Switching DC-DC Converters. *IEEE Trans. Aerosp. Electron. Syst.* **1981**, *AES-17*, 802–808. [CrossRef]
18. Zumel, P.; Ortega, L.; Lázaro, A.; Fernández, C.; Barrado, A.; Rodríguez, A.; Hernando, M.M. Modular Dual-Active Bridge Converter Architecture. *IEEE Trans. Ind. Appl.* **2016**, *52*, 2444–2455. [CrossRef]
19. Qu, L.; Zhang, D.; Bao, Z. Output Current-Differential Control Scheme for Input-Series–Output-Parallel-Connected Modular DC–DC Converters. *IEEE Trans. Power Electron.* **2017**, *32*, 5699–5711. [CrossRef]
20. Fan, H.; Li, H. A distributed control of input-series-output-parallel bidirectional dc-dc converter modules applied for 20 kVA solid state transformer. In Proceedings of the 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–11 March 2011; pp. 939–945. [CrossRef]
21. Chen, W.; Fu, X.; Xue, C.; Ye, H.; Syed, W.A.; Shu, L.; Ning, G.; Wu, X. Indirect Input-Series Output-Parallel DC–DC Full Bridge Converter System Based on Asymmetric Pulsewidth Modulation Control Strategy. *IEEE Trans. Power Electron.* **2019**, *34*, 3164–3177. [CrossRef]
22. Chen, W.; Jiang, X.; Cao, W.; Zhao, J.; Jiang, W.; Jiang, L. A Fully Modular Control Strategy for Input-Series Output-Parallel (ISOP) Inverter System Based on Positive Output-Voltage-Amplitude Gradient. *IEEE Trans. Power Electron.* **2018**, *33*, 2878–2887. [CrossRef]
23. Shu, L.; Chen, W.; Jiang, X. Decentralized Control for Fully Modular Input-Series Output-Parallel (ISOP) Inverter System Based on the Active Power Inverse-Droop Method. *IEEE Trans. Power Electron.* **2018**, *33*, 7521–7530. [CrossRef]
24. Ruan, X.; Chen, W.; Cheng, L.; Tse, C.K.; Yan, H.; Zhang, T. Control Strategy for Input-Series–Output-Parallel Converters. *IEEE Trans. Ind. Electron.* **2009**, *56*, 1174–1185. [CrossRef]
25. Wang, Y.; Guan, Y.; Fosso, O.B.; Molinas, M.; Chen, S.Z.; Zhang, Y. An Input-Voltage-Sharing Control Strategy of Input-Series-Output-Parallel Isolated Bidirectional DC/DC Converter for DC Distribution Network. *IEEE Trans. Power Electron.* **2022**, *37*, 1592–1604. [CrossRef]
26. Jung, C.W.; Lee, D.C. Decoupling Control of Input-Paralleled System with Dual Active Bridge Converters. In Proceedings of the 2019 International Symposium on Electrical and Electronics Engineering (ISEE), Ho Chi Minh, Vietnam, 10–12 October 2019; pp. 226–231. [CrossRef]
27. Lee, S.; Jeung, Y.C.; Lee, D.C. Voltage Balancing Control of IPOS Modular Dual Active Bridge DC/DC Converters Based on Hierarchical Sliding Mode Control. *IEEE Access* **2019**, *7*, 9989–9997. [CrossRef]