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A Space-Borne Ka-Band Tile-Type Phased Array Transmitter Module Based on HTCC Technology

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Abstract: We propose a double-sided layout design method with high reliability for multi-beam phased array transmitter modules based on high-temperature co-fired ceramic technology. Efficient transmission of microwave signals and low-frequency signals is realized by using multi-layer wiring and an inter-layer transition. The proposed Ka-band transmitter module exhibits a gain of ≥26 dB, an output power of ≥21 dBm, and an overall efficiency of the component of ≥40%. The RMS accuracy of phase shift and attenuation is better than 3° and 0.5 dB, respectively. The proposed design method addresses the problems of high integration, lightness, and miniaturization in transmit/receive module design, and shows a good performance of heat dissipation performance and sealing capability. It can be easily expanded to large-scale phased arrays.

Keywords: space-borne; Ka-band; tile-type; phased array transmitter; high temperature co-fired ceramic

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1. Introduction

With the increasing demand for flexible payloads, phased array antennas are developing rapidly [1–4]. Traditional active phased array antenna systems consist of radiating units, transmit/receive (T/R) modules, and beam-forming networks. The interconnection between each functional module is achieved via radio frequency (RF) and low-frequency connectors, which shows the disadvantages of high loss, large footprint, and low integration density [5,6]. With the rapid development of semiconductor technology and micro-packaging technology, highly integrated T/R modules using micro-packaged chips have become the core of active phased array systems [7–11]. Advanced transceiver components mostly use system-in-package (SiP) packaging technology to integrate the chips into one package, which can greatly reduce the size, increase integration density, and reduce interconnection losses [12–14]. With a high-density dielectric substrate as the core, SiP integrates and packages various active and passive components such as RF, analog, and power supply components to build high-performance modules. SiP technology can achieve chip interconnection, heat dissipation, and environmental adaptability protection. Most used high-density substrates include multi-layer printed circuit board (PCB) boards [15] and multi-layer ceramic substrates [16–20]. Due to the unique requirement of space applications, the PCB processing technology cannot achieve flexible signal interconnection between layers. However, ceramic materials, such as low-temperature co-fired ceramic (LTCC) [16–19] and high-temperature co-fired ceramic (HTCC) [20], can achieve multi-layer substrate stacking through multi-layer co-firing technology, enabling flexible interconnection and layout between layers. In the meantime, stacking high-density substrates in the vertical direction and realizing inter-board interconnection through a ball grid array (BGA) can further increase integration density and reduce interconnection length, leading to reduced parasitic capacitance, inductance, and improved RF performance [21].

Plenty of works have been proposed to reduce the footprint of the T/R modules while maintaining good electrical performance, as the size of the T/R module strongly confines

the spacing of radiating elements and the geometry of the active array, which influence the gain and scanning range of the phased array system [2,6]. Van Heijningen et al. [9] proposed a T/R front end based on a gallium nitride (GaN) monolithic microwave integrated circuit (MMIC), which achieved a more compact size compared to traditional T/R modules [7]. However, the proposed MMIC needs to be packaged with a multifunction chip for phase and amplitude control to fully satisfy the requirement of a phased array antenna. Di Carlofelice et al. [10] proposed a compact T/R module with phase and amplitude tuning ability based on 3D packaging technology. However, it consists of two LTCC submodules connected through a metallic interposer board. An additional assembling procedure is needed in the fabrication. Zeng et al. [19] reported a Ka-Band T/R module that integrated four T/R channels into one SiP. This multi-channel T/R module is suitable for large-scale, high-density phased arrays. Currently, most of the T/R modules are designed in a single-sided layout. To further reduce the footprint, designing the SiP in a double-sided way is a promising solution.

In this work, we propose an HTCC-based tile-type four-channel transmitter module for Ka-band phased array antennas. The multi-layer HTCC substrate facilitates signal interconnections, enables self-packaging, and creates cavities for chip assembly. Kovar metal frames are welded on the HTCC substrate for hermetical sealing and signal shielding. The four-channel T/R component features a hermetic metal–ceramic package with a footprint of 12.2 mm × 12.2 mm and a thickness of 4.3 mm, utilizing 169 BGA pins for signal and DC power interconnection and shielding. The HTCC technology enables high integration density, high-reliability hermetic self-packaging, and high RF performance. The distinctive double-sided layout architecture with the combination of the multi-layer routing and the BGA interface enables seamless integration with systems, ensuring optimal input–output port matching and supporting array-scale expansion. The proposed design method also shows the advantages of high consistency and low cost, making it ideal for mass production and use for large-scale phased array systems.

2. T/R Module Scheme

2.1. Brick-Type T/R Module

The brick-type T/R modules combine and integrate multiple transceiver RF channels side by side, as shown in Figure 1. The signal transmission in each channel is planarly interconnected, ensuring good circuit continuity, excellent high-frequency performance, and reliable interconnections. Each channel still maintains a circuit layout similar to a single channel, resulting in a relatively simple circuit design. However, the planar integration density and packaging efficiency are relatively low, leading to the limited scale of the antenna array [22,23]. At the same time, due to the low integration level of the channels, the single assembly process requires mixed assembly of multiple chips on the substrate, which poses challenges for automated assembly production. The common issues encountered by brick-type T/R modules can significantly impact RF performance as operating frequencies increase, especially above the Ka-band.

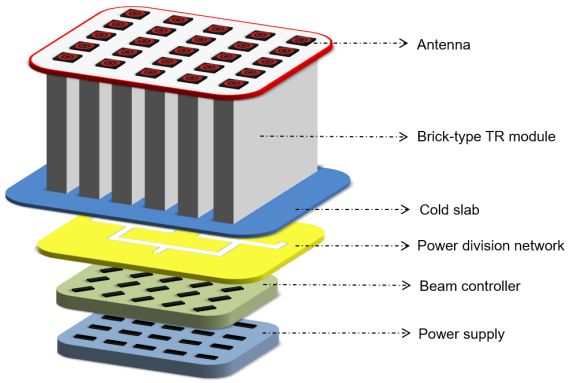


Figure 1. The schematic diagram of brick-type architecture.

2.2. Tile-Type T/R Module

The tile-type architecture is a multi-layer planar structure. The chips in the tile-type transceiver modules are no longer arranged horizontally but arranged vertically in different layers according to function decomposition. Different functional layers are connected through RF vertical interconnection, as shown in Figure 2. Vertical interconnection is the key to the realization of tile-type transceiver components [24,25]. The traditional tile-type architecture relies on structural components and radio frequency connectors for vertical interconnection, making it challenging to ensure high-frequency transmission performance. The external interfaces of the tile-type T/R modules are in the form of connectors, which are not size-efficient. Limited by the antenna array element spacing, the tile-type T/R module design is still challenging. Nowadays, tile-type transceiver modules are designed with multi-layer substrates and three-dimensional integration. The substrates and chips of the tile-type T/R modules are assembled parallel to the array plane, and the signal interconnection between layers is achieved by the quasi-coaxial transition. Usually, chips or circuits with the same functions in multiple channels are integrated in one substrate board. To achieve more complicated functionality, more substrate boards can be used and fastened together to form a complex tile-type sub-array.

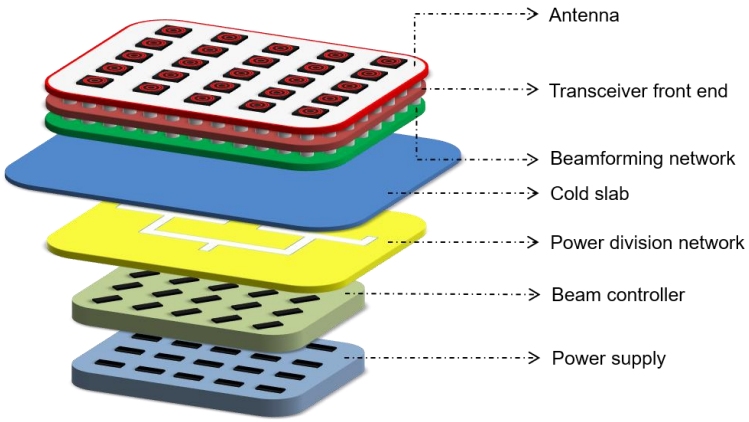


Figure 2. The schematic diagram of tile-type architecture.

It can be seen from the architecture of the active phased array antenna system that tile-type transceiver modules are more suitable for high integration density and low-profile phased array antennas. Compared to brick-type architectures, tile-type systems utilize highly integrated multifunctional chips and micro-assembly techniques to assemble transceiver components in layers and achieve high-density integration, exhibiting the advantages of low profile, light weight, small volume, modularity, and easy scalability. Tile-type architectures are more conducive to system assembly and expansion, especially when the dimensions of the systems are restricted.

3. Tile-Type Transmitter Module Based on HTCC Technology

The proposed Ka-band transmitter module can achieve four-channel signal amplification, with independent control of single-channel amplitude and phase. The key requirements of the performance index are listed in Table 1. These design requirements are decomposed from the link analysis of the phased antenna system, and derived from the requirements of the pointing accuracy of the antenna beam. This design uses HTCC packaging to integrate the active chips on a substrate and transmit signals on different layers of the HTCC substrate. Compared to the traditional single-sided configuration scheme, the new scheme employs the double-sided configuration. On the one hand, it can reduce loss and noise and improve reliability. On the other hand, it makes the component compact in size, light in weight, and flexible in shape. This design requires research on

multiple technologies such as microwave multi-layer substrate production technology, device packaging, and inter-layer vertical interconnection and signal transmission.

Table 1. The main requirements of the transmitter module.

Parameters	Design Requirements
Single channel gain (dB)	≥26
Saturation output power (dBm)	≥21
Efficiency	≥40%
RMS accuracy of phase shift (°)	≤3
RMS accuracy of attenuation (dB)	≤0.5
Inter-channel amplitude consistency (dB)	≤0.5

The HTCC substrate material exhibits excellent resistance to high temperatures, corrosion, and thermal shock, ensuring exceptional stability and reliability. Since multi-layer co-sintering can be achieved, the HTCC process can achieve high-density wiring, thereby improving device performance. Furthermore, HTCC ceramic materials have low insertion loss and high-quality factors, making them suitable for high-frequency applications. Based on the advantages above, the HTCC packaging is used in the proposed design. The characteristics of the HTCC material are listed in Table 2.

Table 2. Characteristics of HTCC.

Characteristic	B210	W412	BX407
Color	black	white	black
Density (g/cm^3)	3.7	3.7	3.7
Permittivity@1MHz	9.7	9.0	10
Dielectric loss angle tangent	3.3×10^{-4}	2.3×10^{-4}	13×10^{-4}
Dielectric strength (10^3 V/mm)	27.8	28	20
Volume resistivity@20 °C (Ω·m)	8.1×10^{13}	8×10^{13}	5×10^{13}
Linear expansion coefficient @40~400 °C ($\times 10^{-6}$ /K)	7.06	7.2	7.5
Thermal conductivity (W/m·K)	17.4	17	13.1
Flexure strength (MPa)	340	370	400
Young's modulus of elasticity (GPa)	280	279	299

3.1. Transmitter Module Scheme Design

The schematic of the proposed transmitter module is shown in Figure 3. The proposed transmitter module is designed for an antenna array or subarray of four radiation elements, so it consists of a four-channel multi-functional chip and four power amplifier (PA) chips. The input signal is pre-amplified and divided into four channels in the multi-functional chip. The amplitude and phase of the signal in each channel can be manipulated independently via the 4-bit digital control attenuators and 6-bit phase shifters, which are integrated in the multi-functional chip. Then the signal is amplified via a PA and sent to the antenna array for transmitting. The proposed scheme ensures the symmetry and ability of independent phase and amplitude control among four channels, which are key features to provide constructive interference in the desired direction, leading to the ability of radiation beam scanning. The configuration of three-stage amplifiers makes a good tradeoff between power consumption and output power.

The link budget analysis is shown in Table 3 with an input power of −5 dBm. The gain or insertion loss (IL) and the saturation output power of each component in the transmitter module are listed in the second and third columns in the table. The signal power at each stage of the link is listed in the fourth column. As the PA works at the saturation state for higher efficiency, the module achieves an output power of 21.2 dBm. The overall link gain can be calculated as 26.2 dB, which satisfies the performance requirements in Table 1.

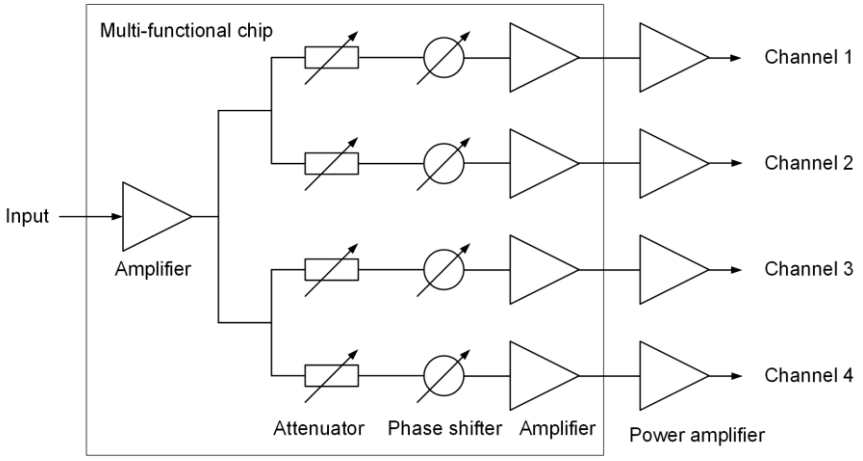


Figure 3. Schematic of the proposed transmitter module.

Table 3. Link budget analysis of transmitter module.

Components	Gain of Components (dB)	Saturation Output Power (dBm)	Signal Power (dBm)
Amplifier 1	16	11.0	11.0
1:4 divider	−7.2	25.0	3.8
4-bit attenuator	−4.0	25.0	−2.2
6-bit phase Shifter	−7.0	25.0	−9.2
Amplifier 2	11.0	5.6	1.8
Power amplifier	21.5	22.0	22.0
Connector Loss	−0.8	30.0	21.2

The core of the transmitter module is a heterogeneously integrated multifunctional chip that consists of a four-channel GaAs chip for phase, and amplitude control and a Si-based CMOS chip that performs multi-channel serial-to-parallel conversion control, electrostatic discharge (ESD) protection, and power-on reset. The fan-in process is used to rewire the bonding points of the CMOS chip, allowing it to be heterogeneously integrated with the GaAs chip, thus combining the performance and size advantages of heterogeneous chips. The schematic of the chip is illustrated in Figure 4.

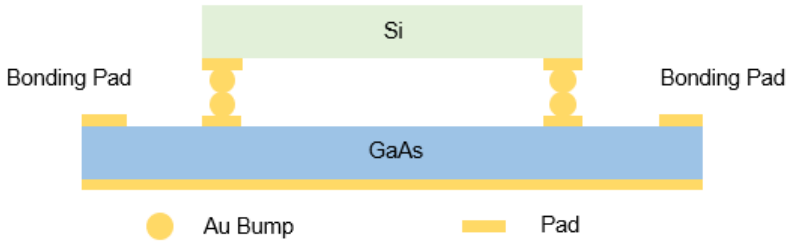


Figure 4. Schematic of the 3-D heterogeneous integrated multifunctional chip.

The transmitter module is based on MMIC technology and HTCC substrate packaging integrated design technology. The schematic of the proposed transmitter module SiP is shown in Figure 5. Step cavities are formed on the substrate for MMIC chip mounting and electromagnetic shielding. A large number of metalized through-holes are designed in the substrate below the chip to achieve good grounding and heat conduction. A number of grounded shielding through-holes are densely distributed around the cavity, and a small metal cover is bonded above the cavity to form an independent cavity structure, which effectively eliminates the spatial crosstalk of electromagnetic signals and the potential instability of the circuit caused by excessive gain in a single cavity. The frame made of

Kovar material is sintered with the substrate, and the cover plate above is sealed and welded in parallel to achieve an airtight seal of all the bare chip cavities. The circuits on the front and back sides are connected through vertical transition inside the substrate. The complex low-frequency wiring and radio frequency interconnections are integrated into the multi-layer HTCC substrate. The interface of the signal and DC power is in the form of a BGA structure.

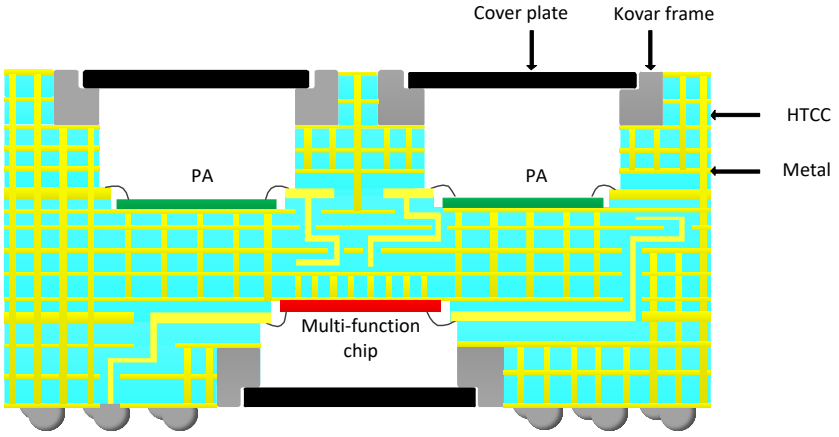


Figure 5. Schematic of the proposed SiP package.

3.2. Key Electrical Structure

3.2.1. Coaxial-Like Transition

The RF signal transmits via coaxial-like transitions between different layers. The schematic of the coaxial-like transition is illustrated in Figure 6. The signal vias act as the inner conductor of the coaxial cable, and the GND vias surrounding the signal vias act as the outer conductor of the coaxial cable [26,27]. As the metalized blind vias can be flexibly fabricated in multi-layer HTCC substrate, the distance between the signal via and the ground via can be adjusted in different layers to achieve a broadband impedance matching in vertical transmission.

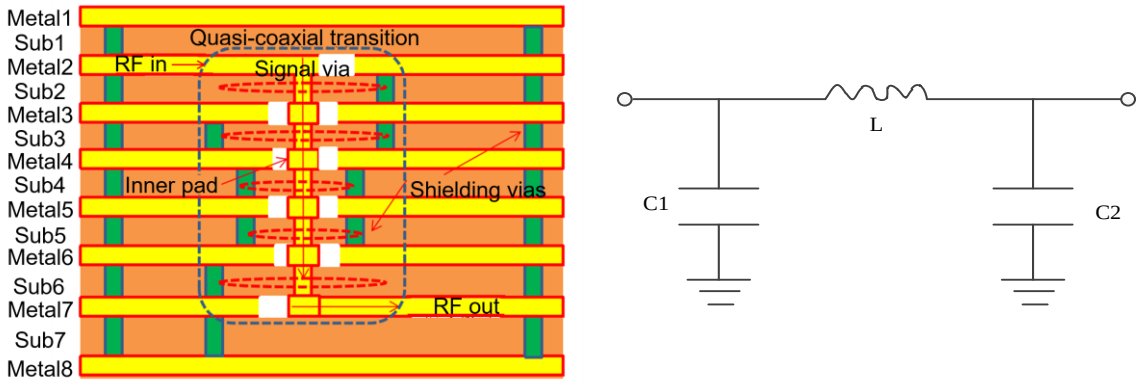


Figure 6. The quasi-coaxial vertical interconnection structure: (**a**) cross-sectional drawing (The yellow layers are metal. The orange layers are substrate. The green vias are shielding vias. The red dashed circles demonstrate that the electromagnetic field is confined by the shielding holes); (**b**) equivalent circuit.

When the ohmic resistance and the conductance can be considered negligible compared to reactance and susceptance, respectively, the impedance of the transmission line can be written as

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \tag{1}$$

where L_0 and C_0 are the series inductance and shunt capacitance per unit length, respectively [28].

When the transmission line is interconnected with the vertical signal through the hole, an extra parasitic inductance ΔL is introduced [29]. The characteristic impedance of the transition structure can be re-written as

$$Z_0 = \sqrt{\frac{L_0 + \Delta L}{C_0}} \tag{2}$$

To compensate for the impedance mismatch caused by the parasitic inductance, an additional capacity ΔC is needed [29]. A general way to introduce compensation capacity is to increase the dimension of the bonding pads at both sides of the vertical transition through the hole. The compensated impedance is written as

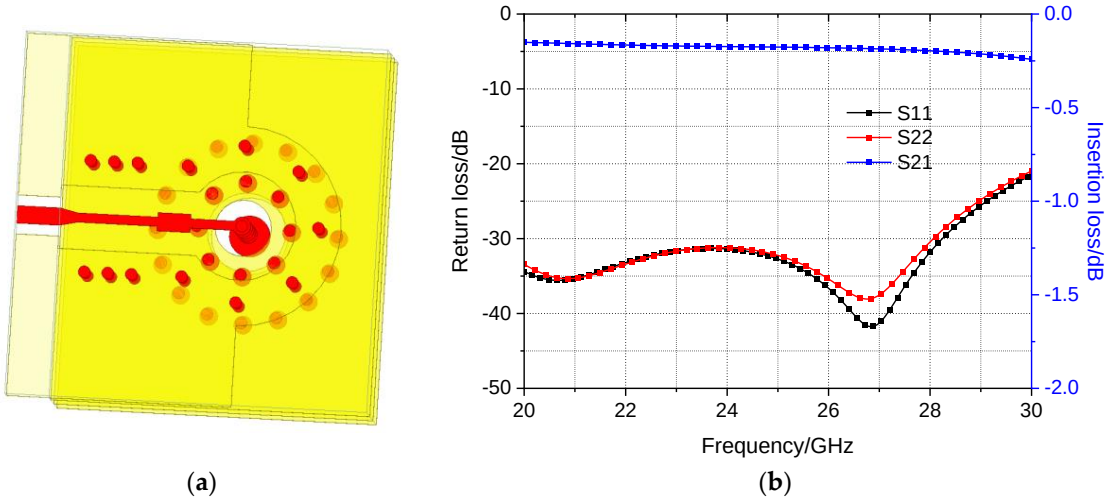
$$Z_0 = \sqrt{\frac{L_0 + \Delta L}{C_0 + \Delta C}} \tag{3}$$

The value of the compensation capacity can be derived from the Equations (1) and (3) as

$$\Delta C = \frac{C_0}{L_0} \Delta L \tag{4}$$

The above formula indicates that by optimizing the matching circuit of the vertical transition, parasitic inductance and capacitance can be effectively compensated for, achieving broad-band impedance matching and improving overall RF performance.

In the proposed design, a stepped impedance transformation structure is employed to achieve broadband matching, enabling the coaxial-like transition to operate effectively from 20 GHz to 30 GHz. To be more specific, the diameter of the GND vias and the width of the transmission line are optimized for broadband matching. The simulation model and results are shown in Figure 7. The return loss is better than 20 dB, and the transmission loss is less than 0.3 dB from 20 GHz to 30 GHz.



(**a**) (**b**)

Figure 7. (**a**) The simulation model of the coaxial-like transition. (**b**) Simulation results of inter-layer vertical interconnection.

3.2.2. BGA Transition

The BGA serves as the interconnection structure between the transmitter module and the PCB network. Similar to the quasi-coaxialstructure in the multi-layer substrate, the BGA structure is composed of a signal solder ball in the center surrounded by the ground solder ball. It can be divided into two parts: the transition from the inside of the HTCC module to the BGA pad on the back of the module, and the transmission from the BGA solder ball to the internal transmission lines of the multilayer PCB. A grounding plane is created around the solder ball. The capacitive effect between the grounding plane and the signal solder ball can be adjusted to match the inductance of the BGA solder ball, thereby achieving a good transmission performance in a wide bandwidth. Another key aspect of this design is ensuring that the diameter of the gap between the grounding plane and the solder ball is less than half the wavelength. If it exceeds half the wavelength, this structure can be equivalent to a loop slot antenna that radiates electromagnetic waves, significantly weakening the RF transmission performance of the transition structure. In essence, the BGA transition structure can be modeled as a coaxial system. By optimizing the size of the ground plane aperture, the spacing between the grounded solder balls, and the dimensions of the solder pads, an effective 50 ohm impedance matching can be achieved.

In the proposed design, the BGA ball with a diameter of 450 µm is used. The simulation model is shown in Figure 8, where the transmitter HTCC module is connected to the PCB via BGA. The inset shows the detail of the BGA transition where the signal solder ball is surrounded by the grounding solder ball, forming a coaxial-like structure. The BGA transition shows a return loss of better than 20 dB, and an insertion loss of less than 0.6 dB in a wide working bandwidth from 20 GHz to 30 GHz.

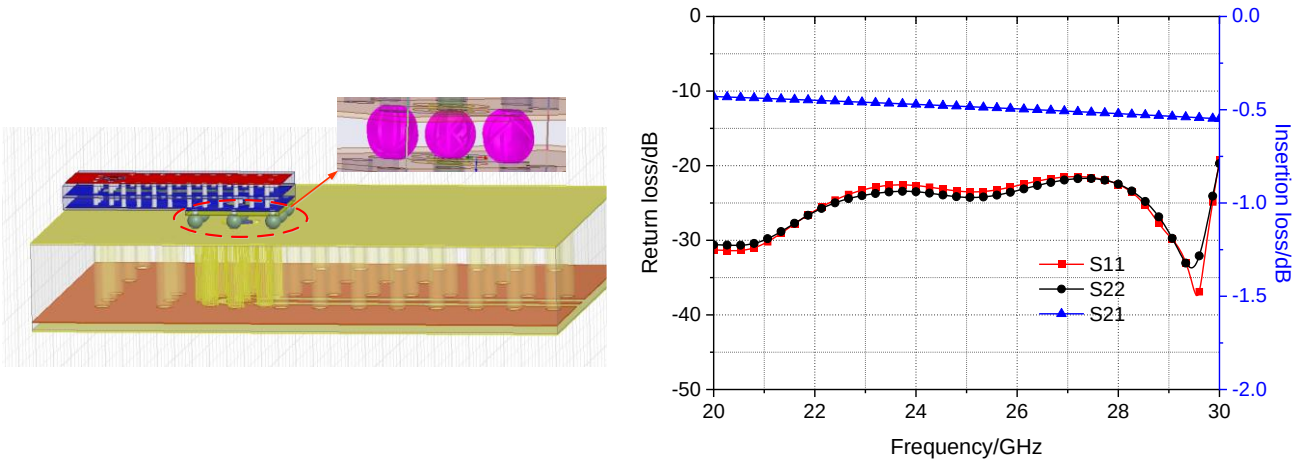


Figure 8. (**a**) The simulation model of BGA transition. (**b**) Simulation results of BGA interconnection.

To ensure assembly accuracy, the tolerance of the shape, cavity, and dimension of the BGA solder pad is strictly controlled. To assess the impact of the fabrication error in the BGA structure, a structure parameter analysis is carried out. The deterioration of return loss with respect to the offset of the solder ball position is simulated, as illustrated in Figure 9. The results show that the return loss is less than 20 dB, even with an offset of 100 µm, which exhibits a good tolerance in fabrication and assembling.

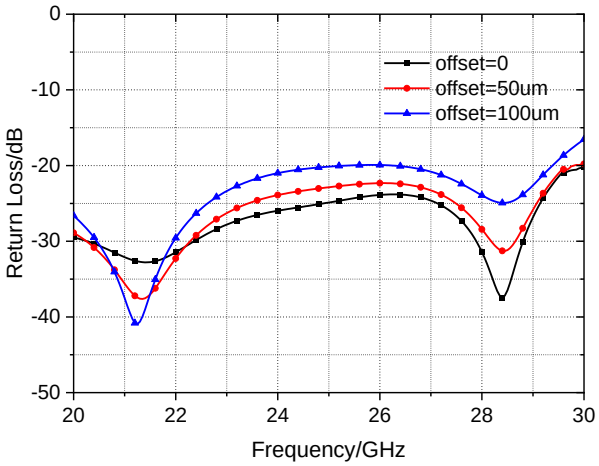


Figure 9. Tolerance analysis of BGA structure.

3.3. Thermal Design

The thermal characteristic of the module is analyzed by the finite element method. To increase the computation speed, some geometrical characteristics of the model are simplified. The thermal analysis is based on a steady-state calculation with conditions of the highest working temperature of 65 degrees at the boundary of the module.

Under the above working conditions, the temperature distribution of each part is calculated. The detailed calculation results of temperature are shown in Table 4. The temperature distribution diagram is shown in Figure 10. The results show that under the calculated working conditions, the temperatures of all devices are lower than the first-level derating value, which verifies the good heat dissipation design of the module.

Table 4. The junction temperature of the active components.

Name	Heat Rate (W)	Thermal Resistance (°C/W)	Shell Temperature (°C)	Junction Temperature (°C)	First-Level Derating Temperature (°C)
Power amplifier	0.233	70	86.1	102.4	115
Multifunctional chip	0.313	80	84.9	109.9	115

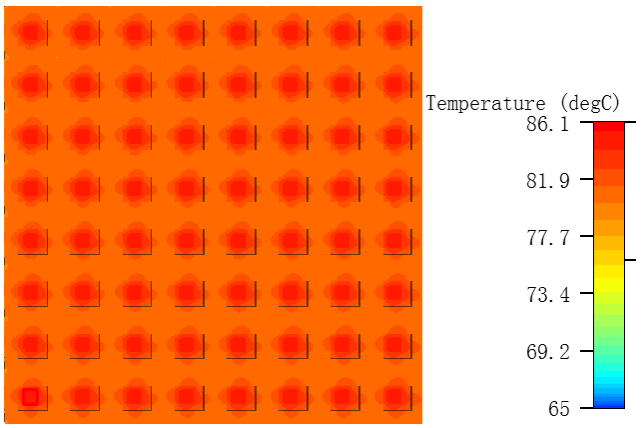


Figure 10. The results of the thermal analysis.

3.4. Reliability Analysis

To ensure high reliability in soldering quality, it is important to predict and analyze the lifespan of the solder ball on the component mounting side. The dimension of the HTCC package is 12.2 mm × 12.2 mm, with a pad diameter of 0.45 mm and a pitch of 0.75 mm.

High-lead solder balls with a diameter of 0.45 mm are used in the BGA structure. The spacing for the most distant signal BGA solder joint is 11.6 mm, while the maximum spacing for BGA solder joints is 15.05 mm. The HTCC module is mounted on a low-loss laminate PCB. The key parameters for lifespan analysis are listed in Table 5. The predicted number of cycles under accelerated thermal stress, N, can be calculated via Equation (5) [30]. Based on the design conditions, the reliability criterion is set to a minimum of 500 temperature cycles, which means the solder joint should be in good condition within 500 temperature cycles. The assessment results indicate that under the conditions of the most distant solder joint, the number of temperature cycles is approximately 554, and the estimated lifespan for the signal solder joint is about 1065 cycles, which verifies the high reliability of the design.

$$N = \left[\frac{0.5\cdot\left(2\cdot\varepsilon_f\cdot h\right)}{F\cdot L_D(\alpha_s\Delta T_s - \alpha_c\Delta T_c)}\right]^{-\frac{1}{c}} \cdot \left[\frac{ln(1-0.01\cdot X)}{ln0.5}\right]^{\frac{1}{\beta}} \quad (5)$$

Table 5. Lifespan prediction calculation process.

Name	Parameter	Furthest Solder Joint	Signal Solder Joint
Fatigue ductility index (for Sn10Pb90, 2 ε ≈ 0.65)	ε_f	0.325	0.325
Height of the solder joint/mm	h	0.45	0.45
Experience coefficient (To match the difference between the idea solder and actual solder joint)	F	1.35	1.35
Distance between the solder joint and the neutral point/mm	L_D	7.53	5.8
Component Substrate thermal expansion coefficient/°C	α_c	5.8×10^{-6}	5.8×10^{-6}
Substrate equivalent thermal expansion coefficient/°C	α_s	1.6132×10^{-5}	1.6132×10^{-5}
Temperature range of the component	ΔT_c	155	155
Temperature range of the substrate	ΔT_s	155	155
Temperature Acceleration Factor	c	−0.39949	−0.39949
Weibull shape parameter	β	4	4
Failure rate	X	25%	25%
Predicted cycles under accelerated thermal stress	N	554	1065

To further assess the reliability of the module, a mechanical analysis is conducted to evaluate the mechanical stress at the BGA solder joint. Assuming the substrate does not undergo bending or warping, and the temperature at each solder joint is the same, the shear strain generated at the solder joint can be expressed as

$$\gamma = \frac{L}{h}(\alpha_b - \alpha_c)(T_{max} - T_{min}) \quad (6)$$

where α_b, and α_c are the thermal expansion coefficients of the PCB and ceramic substrate, respectively. L is the distance from the solder joint to the center. h represents the height of the solder ball; T_{max} and T_{min} indicate the maximum and minimum test temperature, respectively; and γ represents the shear strain at the solder joint [31]. It can be seen from the equation that when the temperature difference, thermal expansion coefficient difference, and solder ball height are constant, the farther the solder joint is from the center point, the greater the shear strain and stress, making the solder ball more prone to deformation.

A mechanical response simulation under load vibration conditions is illustrated in Figure 11. The figure shows the 3D model of the component and the simulated stress at the solder ball. The simulation results indicate that the stress on the solder balls increases gradually from the center of the substrate to the edge of the substrate, and the solder balls at the edge of the module endure the highest levels of mechanical stress. The simulation results are in accordance with the analysis based on Equation (6).

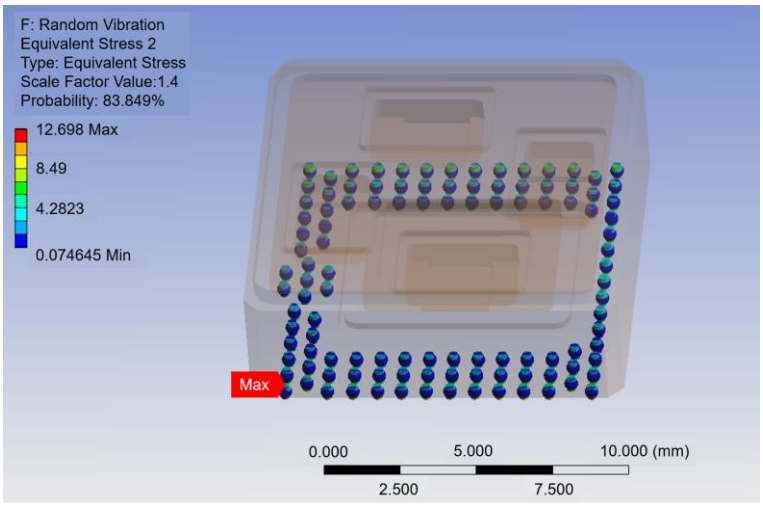
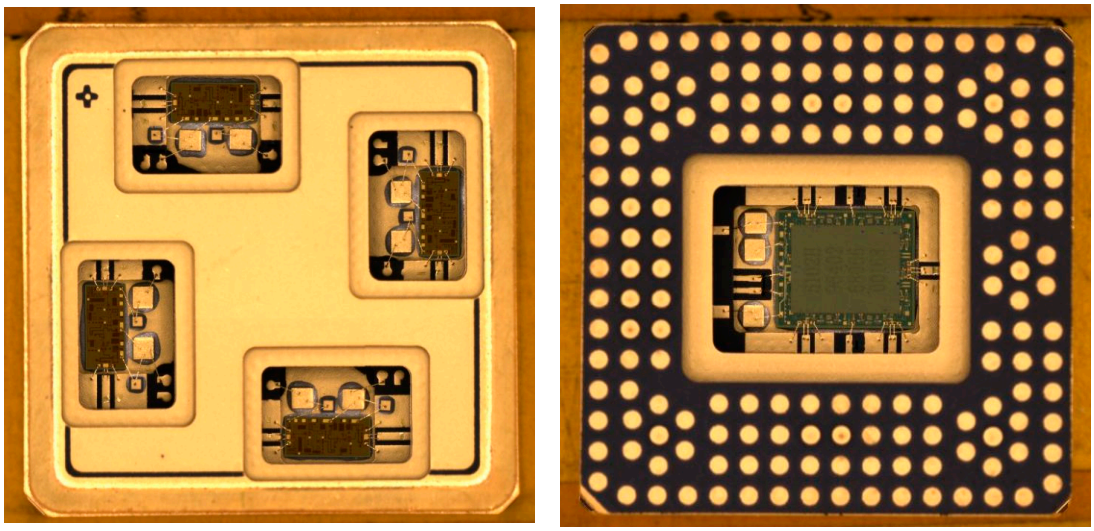


Figure 11. The result of the mechanical response simulation.

4. Test Results and Discussion

A Ka-band miniaturized transmitter SIP module is designed based on the HTCC process. The external interface of this component is in the form of BGA solder balls, making it convenient for surface mounting arrays. It has four-channel phase shifting, attenuation, and amplification functions, and the volume is only 12.2 mm × 12.2 mm × 4.3 mm. Four PAs are mounted at the front side of the module, as shown in Figure 12a, and the four-channel multi-functional chip is assembled at the back side of the module, as shown in Figure 12b.

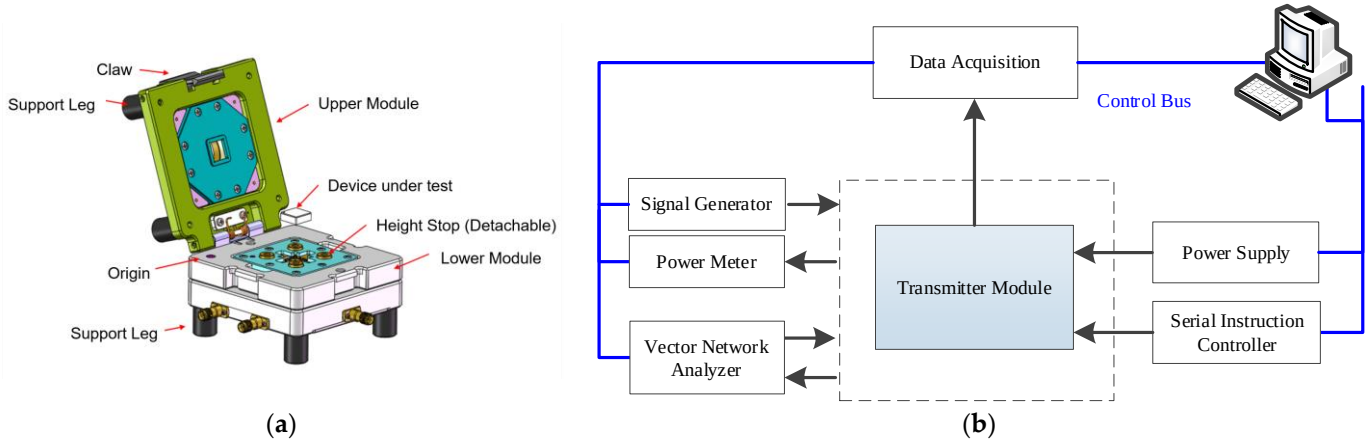


(**a**) (**b**)

Figure 12. The photos of the transmitter module: (**a**) the front side; (**b**) the back side.

The performance of the transceiver module is tested by the setup shown in Figure 13. The HTCC module is mounted on the test fixture to convert the BGA interface of the module into the standard interface of the measurement setup for RF signal and DC power interconnection, as shown in Figure 13a. The module with the fixture is then connected to the measurement setup as illustrated in Figure 13b. The power supply provides +5 V, +3.3 V, and −5 V DC voltage for the active components. The attenuation and phase shifting in each channel are controlled by a serial instruction controller. The gain and the tuning of the attenuation and phase shift are measured by an S-parameter measurement using a vector network analyzer (VNA). The output power is measured by the power meter with a

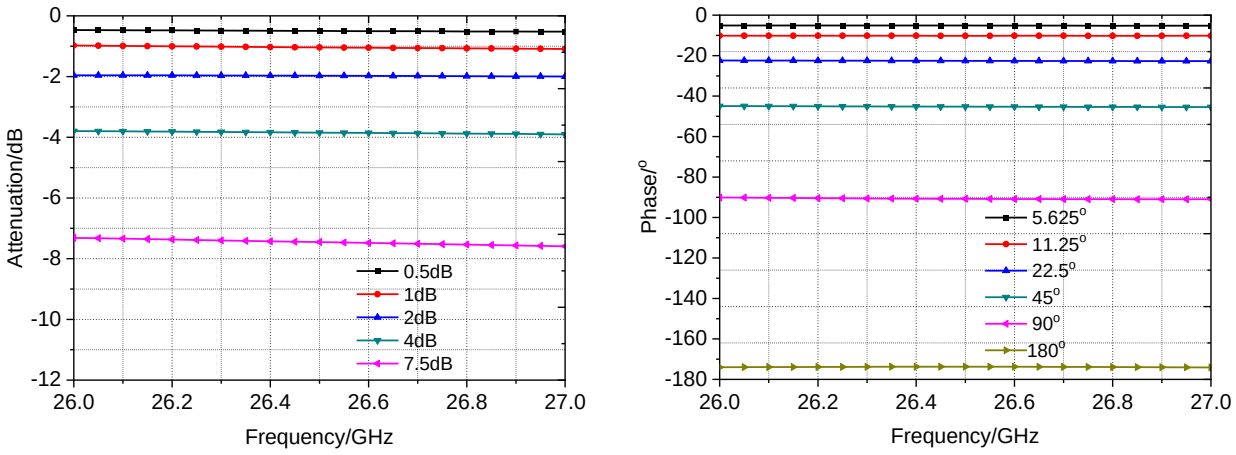
single-tone input from a signal generator. The root mean square resolution of amplitude and phase control is acquired via post-processing of attenuation and phase shifting data. The equipment is controlled by a computer for data acquisition.



(**a**) (**b**)

Figure 13. (**a**) Test fixture for the transmitter module. (**b**) Test setup of the transmitter module.

Firstly, the attenuation and phase tuning performances are measured by a VNA. The VNA is calibrated in the frequency range of 26~27 GHz to calibrate the error and losses in the test equipment and RF cable. Then the transmitter module is connected to the test setup, as shown in Figure 13b. The measurement of attenuation and phase shifting is shown in Figure 14a,b. The attenuation can be increased from 0.5 dB to 7.5 dB with a step of 0.5 dB. The phase shift of the module can be adjusted over 360° with a step of 5.625°.



(**a**) (**b**)

Figure 14. Measurement results of the attenuation and phase tuning performance: (**a**) the attenuation tuning results; (**b**) the phase tuning results.

Then 20 transmitter modules with 80 channels were tested to evaluate the consistency of the proposed design. The measurement results in Figure 15 show that the typical value of the attenuation accuracy RMS is better than 0.5 dB, and the typical value of the phase shift accuracy RMS is better than 3°. The transmitting gain is above 26 dB, and the saturated output power is greater than 21 dBm. The inter-channel consistency of output power is better than 0.5 dB. The efficiency of the module is better than 40%.

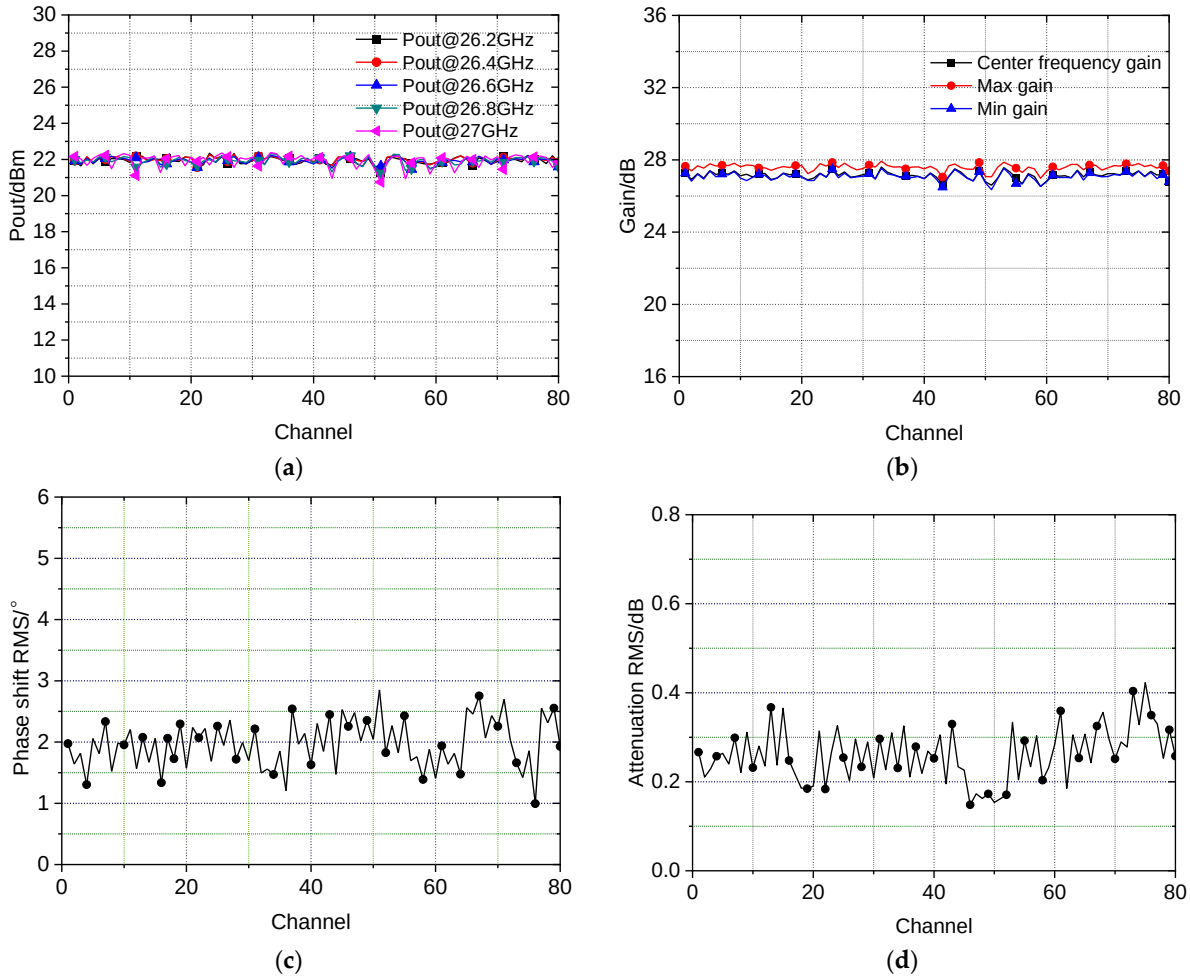


Figure 15. Measurement results of 20 modules: (**a**) the curve of output power; (**b**) the curve of gain; (**c**) the curve of phase shift RMS; (**d**) the curve of attenuation RMS.

A performance comparison is made in Table 6. It can be observed from the table that the proposed module exhibits the highest efficiency with a footprint slightly larger than the T/R module in Ref. [19]. Ideally, the layout of the chips and the routing of the transmission lines can be further optimized to reduce the module size, as the double-sided configuration can provide better space utilization than the single-sided one. Although the output power of the proposed module is smaller than the others in Table 6, it can be improved by using a PA with higher saturation power. The PA in the proposed module is chosen to meet the requirement of the system, as listed in Table 1. The results validate the feasibility of the proposed design for the demand of large-scale active phased array antenna.

Table 6. Performance comparison.

Year	Module	Technique	Size	Pout (dBm)	Efficiency	Layout
2018 [10]	X band single channel T/R module	LTCC, 3D packaging	13 × 16 mm	38	25.9%	2 submodules
2021 [20]	S to X band 4-channel T/R module	HTCC, BGA	27.8 × 27.8 × 12 mm	≥32	-	2 submodules
2023 [32]	Ka-band 4-channel T/R module	Silicon-based MEMs, TSV, 3D integration	18 × 19.5 × 3 mm	≥30	-	2 submodules
2024 [19]	Ka-band 4-channel T/R module	LTCC, BGA, multi-material heterogeneous integration	10.8 × 10 × 3 mm	≥26	≥25%	single-side
This work	Ka-band 4-channel T module	HTCC, BGA	12.2 × 12.2 × 4.3 mm	≥21	≥40%	double-side

5. Conclusions

This work proposed a design for a Ka-band four-channel tile-type transmitter module based on the HTCC process. The presented SiP integrates multiple chips within a footprint of 12.2 × 12.2 × 4.3 mm. The test results show a good consistency among 20 samples. The gain, output power, and overall efficiency of the proposed module exceed 26 dB, 21 dBm, and 40%, respectively. The proposed modules exhibit an RMS accuracy of phase shift of 3° and an RMS accuracy of attenuation of 0.5 dB. The design achieves unique double-sided packaging with a reliable hermetic seal, which enables a compact footprint and conformal integration with systems. This design shows a high integration level and excellent performance, which is very promising in long-lifespan high-reliability space-borne applications.

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References

1. De Gaudenzi, R.; Angeletti, P.; Petrolati, D.; Re, E. Future technologies for very high throughput satellite systems. *Int. J. Satell. Commun. Netw.* **2020**, *38*, 141–161. [CrossRef]
2. Chaloun, T.; Boccia, L.; Arnieri, E.; Fischer, M.; Valenta, V.; Fonseca, N.J.; Waldschmidt, C. Electronically steerable antennas for future heterogeneous communication networks: Review and perspectives. *IEEE J. Microw.* **2022**, *2*, 545–581. [CrossRef]
3. Merino-Fernandez, I.; Khemchandani, S.L.; del Pino, J.; Saiz-Perez, J. Phased Array Antenna Analysis Workflow Applied to Gateways for LEO Satellite Communications. *Sensors* **2022**, *22*, 9406. [CrossRef] [PubMed]
4. Li, M.; Dong, S.; Shi, D. Opportunities and challenges of long-distance high-capacity continuous wireless power transmission. *Chin. Space Sci. Technol.* **2023**, *3*, 1–13.
5. Brookner, E. Developments and breakthroughs in radars and phased-arrays. In Proceedings of the 2016 IEEE Radar Conference, Philadelphia, PA, USA, 2–6 May 2016; pp. 1–6.
6. Latha, T.; Ram, G.; Kumar, G.A.; Chakravarthy, M. Review on ultra-wideband phased array antennas. *IEEE Access* **2021**, *9*, 129742–129755. [CrossRef]
7. Giordani, R.; Amici, M.; Barigelli, A.; Conti, F.; Del Marro, M.; Feudale, M.; Suriani, A. Highly integrated and solderless LTCC based C-band T/R module. In Proceedings of the 2009 European Microwave Integrated Circuits Conference, Rome, Italy, 28–29 September 2009; pp. 407–410.
8. Gryglewski, D.; Rosołowski, D.; Wojtasiak, W.; Góralczyk, M.; Gwarek, W. A 10 W GaN based X-band T/R module for AESA. In Proceedings of the 2016 21st International Conference on Microwave, Radar and Wireless Communications, Krakow, Poland, 9–11 May 2016; pp. 1–4.
9. Van Heijningen, M.; de Hek, P.; Dourlens, C.; Fellon, P.; Adamiuk, G.; Ayllon, N.; van Vliet, F. C-band single-chip radar front-end in AlGaN/GaN technology. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 4428–4437. [CrossRef]
10. Di Carlofelice, A.; de Paulis, F.; Fina, A.; Di Marcantonio, U.; Orlandi, A.; Tognolatti, P. Compact and Reliable T/R Module Prototype for Advanced Space Active Electronically Steerable Antenna in 3-D LTCC Technology. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 2746–2756. [CrossRef]
11. Aljuhani, A.H.; Kanar, T.; Zihir, S.; Rebeiz, G.M. A 256-element Ku-band polarization agile SATCOM receive phased array with wide-angle scanning and high polarization purity. *IEEE Trans. Microw. Theory Tech.* **2021**, *69*, 2609–2628. [CrossRef]
12. Yang, F.; Zhang, B.; Song, L.; Xu, Y. A Compact RF Front-End SiP With Improved Harmonic Suppression for Dual Polarization Phased Array Radar. *IEEE Microw. Wirel. Tech. Lett.* **2024**, *34*, 350–353. [CrossRef]

13. Xu, M.; Liu, Q.; Tang, J.; Wei, Y.; Wei, Z. Design of Tile Integrated Active Array Antenna Based on SIP Module. *Res. Prog. Solid State Electron.* **2023**, *43*, 168–174.
14. Xue, J.; Li, Y.; Shen, X.; Liu, H. Ka-band highly integrated active phased array antenna design based on SIP. *Space Electron. Tech.* **2023**, *20*, 84–88.
15. Xu, H.; Ma, K.; Li, S.; Liu, G.; Wang, Y. A Ka-Band Two-Channel Two-Beam Receiver Based on a Substrate-Integrated Suspended Line. *Electronics* **2024**, *13*, 1582. [CrossRef]
16. Shaik, M.; Agarwal, S.; Pabolu, V. A Miniaturized LTCC RF front-end Module for SATCOM MSS Handheld Terminals. In Proceedings of the 2022 IEEE Wireless Antenna and Microwave Symposium, Rourkela, India, 5–8 June 2022; pp. 1–3.
17. Gao, J.; Yao, X.; Fan, S. Design of a X-band miniaturized T/R module based on LTCC substrate. In Proceedings of the 2022 Asia-Pacific Microwave Conference, Yokohama, Japan, 29 November–2 December 2022; pp. 812–814.
18. Yu, Y.; Chen, Z.; Zhao, C.; Liu, H.; Wu, Y.; Yin, W.-Y.; Kang, K. A 39 GHz Dual-Channel Transceiver Chipset with an Advanced LTCC Package for 5G Multi-Beam MIMO Systems. *Engineering* **2023**, *22*, 125–140. [CrossRef]
19. Zeng, Q.; Chen, Z.; He, M.; Wang, S.; Liu, X.; Xu, H. Design of a Ka-Band Heterogeneous Integrated T/R Module of Phased Array Antenna. *Electronics* **2024**, *13*, 204. [CrossRef]
20. Li, Z.; Sun, H.; Wu, H.; Zhang, S. An Ultra-Wideband Compact TR Module Based on 3-D Packaging. *Electronics* **2021**, *10*, 1435. [CrossRef]
21. Schuh, P.; Sledzik, H.; Reber, R.; Widmer, K.; Fleckenstein, A.; Schweizer, B.; Oppermann, M. T/R-module technologies today and future trends. In Proceedings of the 40th European Microwave Conference, Paris, France, 28–30 September 2010; pp. 1540–1543.
22. Sun, L. A review of antenna-in-package technology for millimeter-wave phased array antennas. *Mod. Radar* **2020**, *42*, 1–7.
23. Wang, Z.; Chen, L.; Yang, T.; Zhang, X. Development and Key Technologies of Spaceborne SAR Active Phased Array Antenna on Integrated Architecture. *Spacecr. Eng.* **2022**, *31*, 126–133.
24. Ma, D.; Yu, C.; Shi, X.; Wang, K. The design of Ka band active array antenna. *Space Electron. Tech.* **2022**, *19*, 90–93.
25. Li, X. Design of a tile-type integrated T/ R module for phased array TT&C system. *Telecommun. Eng.* **2023**, *63*, 125–130.
26. Ding, Y.; Wang, Y.; Xiao, L.; Wang, Q.; Chen, Z. Study on High-Frequency Characterizations of Coaxially Shielded TSV with Mixed Dielectric Layer. *Trans. Beijing Inst. Tech.* **2021**, *41*, 1103–1108.
27. Chen, H.; Li, Q.; Tsang, L.; Huang, C.-C.; Jandhyala, V. Analysis of a large number of vias and differential signaling in multilayered structures. *IEEE Trans. Microw. Theory Tech.* **2003**, *51*, 818–829. [CrossRef]
28. Pozar, D. *Microwave Engineering*, 4th ed.; John Wiley & Sons, Inc.: New York, NY, USA, 2012.
29. Liang, C.; Xie, Y.; Guan, B. *Concise Microwave*, 1st ed.; Higher Education Press: Beijing, China, 2006.
30. *IPC-SM-785*; Standard Only: Guidelines for Accelerated Reliability Testing of Surface Mount Attachments. Institute for Interconnecting and Packaging Electronic Circuits: Bannockburn, IL, USA, 1992.
31. Zhang, C.; Wang, C. Overview on Two Types of Ceramic Array Package and Their Solder Joint Reliability. *Equip. Electron. Prod. Manuf.* **2006**, *68*, 10–17.
32. Yang, D.; Zhao, Y. A Ka Band Four-Channel Short Brick-Type 3D Integrated T/R Microsystem with Silicon-Based MEMS Technology. *IC Des. Appl.* **2023**, *48*, 506–511.