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A Light-Tolerant Wireless Neural Recording IC for Motor Prediction With Near-Infrared-Based Power and Data Telemetry

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Abstract

Miniaturized and wireless near-infrared (NIR) based neural recorders with optical powering and data telemetry have been introduced as a promising approach for safe long-term monitoring with the smallest physical dimension among state-of-the-art standalone recorders. However, a main challenge for the NIR based neural recording ICs is to maintain robust operation in the presence of light-induced parasitic short circuit current from junction diodes. This is especially true when the signal currents are kept small to reduce power consumption. In this work, we present a light-tolerant and low-power neural recording IC for motor prediction that can fully function in up to 300 $\mu W/mm^2$ of light exposure. It achieves best-in-class power consumption of 0.57 μW at 38° C with a 4.1 NEF pseudo-resistorless amplifier, an on-chip neural feature extractor, and individual mote level gain control. Applying the 20-channel pre-recorded neural signals of a monkey, the IC predicts finger position and velocity with correlation coefficient up to 0.870 and 0.569, respectively, with individual mote level gain control enabled. In addition, wireless measurement is demonstrated through optical power and data telemetry using a custom PV/LED GaAs chip wire bonded to the proposed IC.

Keywords

brain computer interface; brain machine interface; neural implant; wireless neural recording; wireless sensor node

I. Introduction

BRAIN machine interface (BMI) or brain computer interface (BCI) has been developed with the initial goal of restoring function for people who are paralyzed, amputated, or

suffer from neuromuscular disorders. Recent research on neural electrode probes [1-7] and neural recording application-specific integrated circuits (ASICs) [7-11] has enabled efficient high-channel recording and decoding along with new findings of various neural features and the development of decoding algorithms. However, the array of wires required for power and data communication and the bulky form factor of the neural recording ASICs has limited the use of conventional high-channel recording systems [7-11]. Although flexible electrode wires [5-7] alleviate some of the challenges, the associated tethering forces increase the risk of scar tissue and thus prevent safe and long-term monitoring of neural activity.

To address this challenge, different free-floating neural recorders have been proposed with miniaturized size, a characteristic critical to achieving dense recording sites and minimum brain damage. These miniaturized standalone free-floating motes include only single channel per mote rather than multi channels with denser array of electrodes. While the latter approach can achieve very small intra-mote channel pitch, the chip size needs to be increased accordingly, hence results in similar average pitch between channels. Therefore, in terms of acquiring multiple independent sources of information, regular spacing of the single-channel free floating motes is preferable to supersampling small spatial regions with wide gaps between groups of channels of multi-channel free floating motes. A near-field RF-based neural grain [12,13] is one such system. The neural grain records electrocorticography (ECoG) signals with near-field RF-based power transfer and bidirectional communication. In [13], *in vivo* measurement with multiple implanted neural grains is demonstrated; however, the remaining challenge is that 0.5W of transceiver (Tx) power is required to operate 0.5 × 0.5mm RF-based neural grains, which exceeds the safety regulations by 10× [12]. Another approach utilizes ultrasound for wireless power transfer and data link. [14] introduces an ultrasound-based neural dust that adopts amplitude modulation (AM) backscattering for data telemetry, achieving low nonlinearity below 1.2%. However, it requires a 0.75 × 0.75×0.75mm bulky piezoceramic, which results in an overall dust size of 0.8 mm^3. Alternatively, in [15,16], a near-infrared (NIR) light is exploited for power and data telemetry using a custom photovoltaic (PV) cell and light-emitting didoes (LED). The NIR-based neural recorder reported in [15] achieves the smallest size, 0.25 × 0.06mm, reported to date among state-of-the-art standalone free-floating neural recorders. However, lacks data downlink capability and the surface electrode of the mote only allows surface potential monitoring or injection of the whole mote into brain tissue, which can cause bleeding or tissue damage.

In [16], a 0.74μW 0.19×0.17mm NIR-based wireless neural recorder with random chipID [17] and on-chip neural feature extraction is proposed. It is designed based on the two-step wireless neural recording concept described in Fig.1. In the envisioned system, numerous free-floating motes are placed in the sub-dural space to record neural activities, while only carbon fiber electrodes with less than 10μm diameter [18] penetrate several mm into the brain tissue. As the carbon fiber electrodes have been shown to incur minimal chronic scar formation [18], the proposed system can improve the long-term sustainability significantly. A repeater unit in the epidural space (Fig.1, center) powers and programs free-floating motes by emitting 850 nm NIR lights. A custom dual-junction PV layer on top of the CMOS circuit layer of the free-floating motes harvests the energy. At the same time, the optical receiver (ORx) translates light modulation into digital data. A custom micro-LED transmits

data by firing LED pulses so that the repeater unit receives the pulses emitted from multiple motes using an array of single-photon avalanche diodes (SPAD) to decode them using the random chipIDs of the motes.

This work uses the same system architecture as that proposed in [16] and builds on it by proposing a new CMOS circuit layer that addresses the challenge of light tolerance. Although most of the perpendicular light used to power the motes is absorbed by the GaAs-based PV layer [19] that sits on top of the CMOS circuit layer, the reflected and scattered 850nm NIR light still can penetrate through the sidewalls of the free-floating motes (Fig.2), impacting overall circuit performance. Furthermore, the sub-μW circuit with limited supply current is particularly susceptible to light-induced parasitic short-circuit currents. In conventional chip packaging, the light can be blocked using an opaque encapsulant, whereas NIR-based free-floating motes need the PV layer and LED exposed to the light for wireless powering and data communication. A partly transparent encapsulation that exposes the PV layer and LED only and blocks light for the CMOS circuit layer is problematic for sub-mm-level packaging. Therefore, a light-tolerant circuit design is essential for the robust operation of the envisioned neural recording system.

To address this challenge, we proposed a light-tolerant neural recording IC for NIR-based free-floating motes that wireless operate under 150μW/mm^2 of target optical power density [20]. It achieves light-robust operation up to 300μW/mm^2 of NIR light power density, whereas the baseline implementation fails at 8 μW/mm^2[16]. In addition, the proposed design includes on-chip feature extraction and individual mote-level gain control capability with an overall power consumption of 0.57μW, which is the lowest among state-of-the-art free-floating motes [13-16].

This article is organized as follows. Section II provides the system overview and discusses the light robustness. Section III describes the light tolerant circuit implementation. Section IV presents the measurement results, and Section V concludes this article.

II. System Overview and Light Robustness

A. System Overview

The circuit diagram of the proposed neural recorder is illustrated in Fig. 3. The main signal chain is composed of three stages: neural signal acquisition, neural feature extraction, and data transmission. The neural signal acquisition block consists of a three-stage bandpass low-noise amplifier to acquire single neuron-level spikes that are probed by the carbon fiber electrode [18]. It also passes the signal with the frequency band of interest through precise bandpass filtering. In this work, we focus on the 300–1000Hz band to extract a neural feature called spiking band power (SBP) [21-23]. SBP is defined as the absolute average of the signal amplitude in the 300–1000Hz band, and this neural feature is known for achieving high motor prediction accuracy relative to a standard 7.5kHz high bandwidth neural recording despite its low bandwidth output [21-23]. By computing the SBP on-chip, the data uplink communication bandwidth is reduced to a maximum of 100s of Hz, thereby saving uplink power and uplink channel capacity. Furthermore, the SBP is computed with energy- and area-efficient circuits (described in Section III). The acquired SBP data

is encoded in symbol-interval modulation (SIM) of uplink LED packets to avoid data conversion overhead. A single uplink LED packet consists of 16b pulse-gap modulated (PGM) data including the random chipID [17].

Thanks to the dual-junction PV cell of the custom GaAs chip [19], 1.5–1.6V of supply voltage is directly supplied to the chip, eliminating on-chip DC-DC conversion overhead. The vertically stacked dual junction PV cell in [19] have junctions with the identical GaAs-based materials and bandgap energies. It is designed to achieve equal optical absorption at each of junctions doubling the voltage output while reducing the number of lateral series connections and shunt leakage paths. The PV cell generates I_{SC} = 1.1μA and V_{OC} = 1.6V at 150μW/mm^2 of target 850nm NIR light power density, where 190 μW/mm^2 is the maximum NIR optical power density for human dura as evaluated in [19]. In addition, AC modulation of the NIR light power is translated into digital modulation by ORx to execute clock and data recovery (CDR). The clock recovery circuit locks the on-chip clock to the modulation frequency of the light. This recovered clock is used to set an accurate corner frequency of the bandpass transfer function of the amplifier chain using the bias currents generated from the switched capacitor. Note that the clock recovery is done globally at the initial start-up phase of the multiple probes. It makes an array of probes to be locked to the same target frequency, therefore, the corner and the bias current of each probe can be set accurately based on their recovered frequency, minimizing the impact of process and voltage variation across probes. The data recovery block receives the serial data from the pulse width modulation (PWM) of the NIR light and programs the chip configurations including the gain setting of the amplifier and SBP extraction unit.

B. Light Induced Current and Light Robustness

Unlike conventional chip design with opaque encapsulation, the proposed system must maintain its performance under the condition where NIR photons invade from the sidewall and bounce around the CMOS layer. Basically, when photons hit any p-n junction within the CMOS circuit layer (Fig. 2), the light-induced carriers by the p-n junctions cause a movement of holes to the p-side and electrons to the n-side, which is known as a photovoltaic effect [24]. In other words, every p-n junction may act as a small solar cell that generates short-circuit current (I_{SC}) that is proportional to the light power intensity and junction area [25]:

$$I_{SC} = SR \cdot P_{NIR}(\lambda) = \left(\frac{q\lambda}{hc}\right) EQE \cdot I_{NIR}(\lambda) \cdot A_{junc} \quad (1)$$

where SR is spectral responsivity, EQE is the external quantum efficiency, I_{NIR} is NIR light intensity, and A_{junc} is the junction surface area. Any conducting path in the proposed system, especially for analog blocks with high impedance paths, can be affected by the parasitic light-induced short-circuit current (I_{SC_P}). If there is any I_{SC_P} flowing in or out of the conducting path between node X and node Y, we define the light robustness coefficient (LRC) of the conducting path as follows:

$$\alpha_{LR} = \left(\frac{I_{XY}}{\sum I_{SC\_P}}\right) \cdot \left(\frac{1}{V_{XY}}\right) = \frac{G_{XY}}{\sum I_{SC_P}} [V^{-1}] \quad (2)$$

where I_{XY}, V_{XY}, and G_{XY} are, respectively, the original conducting current, the voltage difference, and the conductance of the path between node X and Y when there is no light at all. If a conducting path has significantly high conductance over the sum of I_{SC_P} in the path, then the path is barely impacted by the light and therefore achieves high light robustness (high α_{LR}). On the other hand, if a path has low α_{LR}, it is susceptible to light. One example is a capacitive amplifier with the feedback resistor R_{FB} (Fig. 4). In many applications including neural recording or biomedical sensing, a high R_{FB} (or low G_{FB}) is required to achieve a low high-pass corner frequency (f_{HP}). In conventional designs with opaque encapsulation, total I_{SC_P} is zero, so no consideration of α_{LR} is needed. However, in the proposed NIR-based neural recorder, it is critical to implement a high R_{FB} in the neural amplifier chain while simultaneously achieving a high α_{LR}, a feat that is very challenging. The proposed neural recorder is designed with the consideration of α_{LR} in every building block to achieve overall light robustness of the system.

III. Circuit Implementation

A. R_{PSD}-less Neural Amplifier

A pseudo resistor, R_{PSD}, is frequently used for DC biasing or feedback of the amplifier (Table I, left) of a miniaturized neural recording IC [15, 16] since it can easily achieve over a few TΩ of high impedance with only a few transistors, which results in an overall compact layout area. However, R_{PSD} not only has poor process sensitivity but also cannot avoid an extremely low α_{LR} (Table I, left). With R_{PSD}, the DC-bias level drifts at < 1μW/mm^2 of light intensity in simulation, whereas we need a R_{FB} that can sustain at least 150μW/mm^2 of light intensity.Light tolerance of R_{PSD} based structure can be improved using photo induced current compensation technique [26], however, the high process sensitivity of R_{PSD} still remains as a main challenge using R_{PSD} as R_{FB}. Another R_{FB} type adopting a series-to-parallel switched capacitor was introduced in [27] and improves process sensitivity. Thanks to its higher G_{FB}, the series-to-parallel switched capacitor achieves significantly higher α_{LR} than R_{PSD}; however, its high number of switches results in a large total junction area and high I_{SC_P}, and thus α_{LR} is still too low (Table I, middle). In this work, we designed a 3× voltage attenuator and increased the input and the feedback capacitor by the same factor to maintain the f_{HP} similar to the series-to-parallel switched capacitor approach, as shown in (3) and (5).

$$\begin{aligned} f_{HP,\,s-to-pCs} &= \frac{1}{2\pi} \cdot \left(\frac{C_s f_{CLK}}{10}\right) \cdot \frac{1}{C_n} \\ &= \left(\frac{1}{20\pi}\right) \cdot \left(\frac{C_s}{C_n}\right) \cdot f_{CLK} \end{aligned} \quad (3)$$

$$G_{FB,\,s-to-pCs} = \left(\frac{1}{10}\right) \cdot C_s f_{CLK} \tag{4}$$

$$\begin{aligned} f_{HP,\,proposed} &= \frac{1}{2\pi} \cdot \left(\frac{C_s f_{CLK}}{3}\right) \cdot \frac{1}{3C_n} \\ &= \left(\frac{1}{18\pi}\right) \cdot \left(\frac{C_s}{C_n}\right) \cdot f_{CLK} \end{aligned} \tag{5}$$

$$G_{FB,\,proposed} = C_s f_{CLK} \tag{6}$$

While maintaining a similar level of f_{HP}, the proposed approach achieves around $10\times G_{FB}$ compared with series-to-parallel switched capacitor-based approach, as shown in (4) and (6), while having a lower I_{SC_P} resulting a $5{\cdot}10^4\times$ and 46 × improvement in α_{LR} compared with R_{PSD}-based and series-to-parallel switched capacitor-based approach, respectively (Table I).

In this work, we propose a three-stage neural amplifier composed of a low-noise amplifier (LNA) followed by two programmable-gain amplifiers (PGAs) (Fig. 5, top). The gains of the LNA and feedback attenuators of LNA and PGA1 are set by the transconductance (g_m) ratio as shown in the bottom of Fig. 5 to avoid large area occupation of capacitors in the conventional capacitive amplifiers [28]. Operational transimpedance amplifier (OTA) in [28] with an inverter-based input stage is implemented with cascode N/PMOS transistors included in both input and output stage of the OTA (Fig. 5, bottom). In subthreshold region, g_m is proportional to bias current, therefore, the OTA gain can be accurately controlled by bias current ratio of input and output stage. Power consumption of each attenuator is 19.4nW (5.4% of the total amplifier) providing sufficient bandwidth for constant attenuation across the main signal bandwidth, whereas noise contribution of the attenuators is negligible compared to thermal noise of effective R_{FB} located at the same noise transfer path of the attenuators. Area overhead of the proposed structure mainly comes from the MIM and MOM combined input capacitor C_1 (6.9pF), while C_2 and C_3 are only 0.4pF and 2.5pF, respectively (Fig.5). The amplifier achieves 23MΩ of input impedance at 1kHz, which is an order of magnitude larger than the 1kHz impedance of the carbon fiber electrode which varies from sub-MΩ for short-term implant to few-MΩ for long-term implant [18].

The differential-to-single-ended PGA2 implements a simple switched capacitor resistor for R_{FB} to set the f_{HP} of the overall transfer function of the amplifier chain. In PGA2, the proposed 3× feedback attenuator + 3× input and feedback capacitor scheme are not required since the simple switched capacitor resistor already satisfies high α_{LR} and the target f_{HP}. PGA2 also operates as a gm-C filter that sets a low-pass corner frequency (f_{LP}) of the amplifier chain. As the amplifier operates in the sub-threshold region, the transconductance is defined as follows:

$$g_m = \frac{I_{DS}}{nV_T} \tag{7}$$

where I_{DS}, n, and V_T, are the drain-to-source current, subthreshold slope, and thermal voltage, respectively. The I_{DS} is set by I_{REF} generated by the switched-capacitor-based G_m biasing circuit; therefore, it is proportional to the switching capacitance, C_{SW}, and frequency.

$$I_{DS} = m \cdot I_{REF} = k \cdot C_{SW} \cdot f_{CLK} \tag{8}$$

From (3) and (4), the bandwidth of the gm-C filter is precisely defined by the capacitance ratio and clock frequency:

$$f_{LP} = \frac{g_m}{C_L} = \left(\frac{k}{nV_T}\right) \cdot \left(\frac{C_{SW}}{C_L}\right) \cdot f_{CLK} \tag{9}$$

Therefore, both f_{HP} and f_{LP} are set by the capacitance ratio and f_{CLK} recovered from the CDR. Amplifier DC offset is cancelled from stage to stage by AC coupled capacitors, while the inner stage input offset is mitigated by the feedback loop gain.

B. Neural Feature Extraction Unit

Given the extremely small power budget, we focus on the low bandwidth neural feature called SBP for the motor function decoding to minimize the power consumption. In a conventional approach, SBP, which is defined as the absolute average of signal amplitude in the 300–1000Hz band [21-23], is extracted using high-power ASICs to record a raw high bandwidth neural signal and then filter it in the digital domain and perform absolute integration (Fig. 6). Instead, we introduced an energy-efficient and compact on-chip SBP extraction in the an alog domain using the charge integration described in [16]. However, the analog domain SBP extractor in [16] relies on only tens of pA of on current to charge an integration capacitor, which is susceptible to I_{SC_P}. In this work, we propose an area- and energy-efficient, light-tolerant digital SBP extraction unit using a 2.8-bit flash-ADC and pulse-counter-based integrator as shown in Fig. 7(a). The proposed unit consists of a V_{REF} generator implemented with a diode stack (12nA in simulation) and dynamic comparators operating with staggered clock signals with six different phases, followed by pulse generators. Thanks to the staggered clock signals with six different phases, all the evaluation edges ($EV_{[5–0]}$) are non-overlapped. Therefore, the time domain integration of the absolute amplitude could be done by simply combining six output pulses ($P_{[0–2]}$ and $N_{[0–2]}$ in Fig. 7(a)) by logic gates and counting them by a single shared asynchronous counter. As a result, the total quantized area of the AMPOUT signal in Fig. 7(b) is encoded in the time interval as the LED_EN, which triggers the firing of an LED packet for data uplink. The threshold count N_{TH} in Fig. 7(a) can be updated to control the gain of the SBP extraction unit. All the components, including the V_{REF}generator, the dynamic comparators, and the digital circuits implemented with standard cells, meet the high α_{LR} standard for light-robust operation. The dynamic comparators and digital standard cells have high drivability during transition phase and strong retention in steady state significantly enhancing the light tolerance. V_{REF} generator is designed with sufficient supply current of 12nA at the typical corner and 2.7nA at the worst corner (simulation) to handle sub-nA

level of total I_{SC_P} with enough margin. The process variation and mismatch impact of the output voltage of V_{REF} generator on overall decoding performance and SBP extraction is minimized by two main factors. First, the decoding accuracy and SBP is highly correlated to the input spiking rate rather than the linearity of the signal amplitude. In addition, a single step of the quantized voltage, ΔV in Fig.7 (b), is 130mV, whereas its standard deviation across both process variation and mismatch is 6.2mV (MC simulation with 1000 samples) minimizing linearity degradation.

C. Optical Receiver (ORx)

An ORx is a key component for data downlink converting AC modulation of the NIR light intensity to the digital sequence that is needed for CDR. The main challenge of ORx is to receive low frequency data modulated through the supply without having any low impedance path which is susceptible to light (poor a_{LR}). In this work, we propose a novel ORx utilizing a high pass filter whose cut-off frequency is much higher than the modulation data rate by combining it with the hysteresis comparator. The ORx is composed of dual 2T-VRs [29]: one AC-coupled to $V_{DD}$and another to ground and a hysteresis comparator (Fig. 8). The 2T-VRs are sized for 1.4nA of current in simulation to ensure high a_{LR}, and the RC-time constant is set much shorter than the light modulation period but, still longer than the time constant of the hysteresis comparator. Therefore, the proposed ORx fetches the input modulation and maintains the output value until the next toggle.

D. Pulse Gap Modulator and LED driver

The data transmission block, including PGM and an LED driver, receives the output of the SBP extraction unit and emits light using LED to the repeater unit. PGM encodes the 10b random chipID [17] and 6b AFE gain configuration (3b for the amplifier and 3b for the SBP extraction unit), 17 pulses total where the 16 pulse gaps of either $2T_{CLK}$ or $3T_{CLK}$ stand for data 0 or 1, respectively (Fig. 9). The 6b AFE gain configuration in the uplink LED packet lets the external users know the current gain status and acts as an indicator of successful data recovery, which will be covered in Section III.E.

The custom LED [19] requires mA-level driving current to maximize external quantum efficiency (1% EQE at 0.1mA and 2% EQE at 1mA) and to maximize the detection rate of the repeater. However, the supply current of the chip is limited by the short-circuit current that the PV cell can generate (I_{SC} = 1.1μA at 150μW/mm^2 of NIR light [19]). Therefore, we slowly charge three capacitors in parallel during the LED off time and up-convert the voltage using the series connection of three capacitors to provide instinct high driving voltage and current on LED ($V_{LED,PK}$ = 2.15V, $I_{LED,PK}$ = 3.73mA in simulation). The proposed PGM provides $2T_{CLK}$ of long capacitor charging time of the LED driver, and this helps the LED driver to reduce the charging current level. LED_EN from the SBP extraction unit toggles the 17 PGM LED light pulses, and the extracted SBP is encoded in the time interval between two adjacent LED_EN signals or two LED packets (Fig. 9(b)). This modulation s cheme is referred to as PGM-based symbol interval modulation (PGM-SIM).

E. Clock and Data Recovery (CDR)

In Fig. 10, a block diagram of the proposed CDR is introduced. In the power-on reset phase, a default clock generator sends out default clock to the overall system, and the system enters the clock recovery phase. With the external NIR light modulated at a constant frequency of 8kHz, the clock recovery block calibrates the digitally controlled oscillator (DCO) with a 4b-thermometer-coded control scheme to match the received modulation period with the DCO period (Fig. 10). After the DCO frequency is calibrated, the LOCK signal rises and switches the system clock from the default to the recovered clock using glitch-free multiplexers.

After the clock recovery phase, the system functions normally with the data recovery triggered whenever the passcode is received. The repeater unit programs the system by modulating the NIR light intensity with a pulse-width modulation (PWM) scheme, and it sends a total of 37 bit data composed of 18 bit for passcode and 19 bit for the system configuration (Fig. 10). There are two types of passcodes implemented: global and local. A global passcode is an 18 bit, fully hardwired code that is identical for every recording chip. Therefore, if the repeater sends out a particular configuration with the global passcode, all the free-floating motes under the receiver update their configurations to the identical setup with a single programming. On the other hand, a local passcode is composed of an 8 bit preamble plus 10 bit random chipID [17]. This allows individual remote gain control (RGC). Depending on the obtained neural signal magnitude at each mote, the repeater layer can program an individual chip without affecting other motes. This RGC capability enables flexible channel gain adaption, for instance, off-chip-level automatic gain control (AGC) by monitoring the average LED firing rate of every channel.

IV. Measurement Results

The proposed light-tolerant neural recording IC was fabricated in 180nm CMOS (Fig. 11). The chip can fully function under 300μW/mm^2 of NIR optical power density, which exceeds the target optical power density for the real application (150μW/mm^2). AFE performance was measured with a bare die exposed to NIR light, and a wireless measurement was performed by using a commercial NIR light source for power transfer and downlink. A commercial SPAD was used to receive uplink signals sent by the LED. In this setup, the proposed IC was wirebonded with a custom PV/LED GaAs chip side-by-side without any other tethering wires. In addition, *in vivo* measurements were performed by connecting a carbon fiber inserted into the brain of an anesthetized Long Evans rat. Furthermore, a 20-channel prerecorded motor cortex signal acquired by Utah microelectrode arrays was provided to the chip after the proper attenuation to emulate the *in vivo* measurement. Then, the finger movement of a monkey was predicted using the resulting SBP produced by the proposed IC.

A. AFE Performance under Bare Die Exposure to NIR Light

For AFE performance validation, the bare die was exposed to a commercial 850nm light source (IRS4, CMVision) and the measurement was performed in a temperature chamber maintaining 38°C. The amplifier achieves 68dB peak gain with an SBP bandwidth range

of 380 to 1060 Hz under 150μW/mm^{2}NIR light which is sufficient to amplify and filter hundreds $\mu V_{pk-to-pk}$ of input neural spike in interest and to fully utilize the available voltage headroom of the chip. The common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) were higher than 67dB. The measured input referred noise (IRN) was 6.2μV_{RMS}. The difference of the measured performance was negligible when the 850nm NIR light source with the target NIR optical power density 150μW/mm^2 is turned on and off (Fig. 12, Table II). Fig. 13 shows the measured peak gain and f_{HP} across the NIR light intensity level for an R_{PSD}-based baseline and the proposed structure. While the baseline structure failed at 8μW/mm^2, the proposed structure remained stable up to 300μW/mm^2.

Fig. 14 demonstrates the measured transient waveform of the fully functioning AFE with the 300μW/mm^2 NIR light turned on. The pre-recorded motor cortex signal of a monkey was streamed into the chip using an arbitrary waveform generator (AWG, Keysight, 33600A) and 1000-to-1 on-PCB attenuator. AMPOUT at the second row is the output of the amplifier and, at the same time, the input of the SBP extraction unit. $P_{[0–2]}$ and $N_{[0–2]}$ are the outputs of the six pulse generators in Fig.7. The LED_EN signal is the final output of the SBP extraction unit. The proposed computing unit consumed 29.5nW in simulation while occupying only 0.045mm^2.

B. Wireless Optical Measurement

To validate the wireless optical function, the proposed IC was wire bonded to the custom PV/LED GaAs chip [19] and measured with the fully wireless optical setup including 850nm laser (QFLD850200S, Qphotonics) for NIR powering and data downlink. A SPAD detector was used for uplink reception (SPDOEMNIR, Aurea) (Fig. 15). The measured transient waveform of the optical downlink using PWM of the external light is presented in Fig. 16. The V_{DD} node was monitored through the on-board analog buffer and plotted in the second row of Fig. 16 while modulating 850nm light intensity between 500 and 0 μW/mm^2. Note that CDR (32ms for CR and 70ms for DR) occurs only once at start-up or very infrequently staying most of time in nominal operation phase under 150 μW/mm^2, therefore, 500μW/mm^2 peak modulation density for CDR does not impact tissue overheating. ORx captures and translates the V_{DD} modulation into the digital signal. When it detects the 18b local programming passcode (8b preamble + 10b chipID), the VALID signal rises, and the data recovery of the 19b-chip configuration is executed.

With the identical optical setup in Fig. 15, the wireless data uplink functionality was validated (Fig. 17). The pre-recorded motor cortex signal of a monkey was streamed into the chip using an arbitrary waveform generator (AWG, Keysight, 33600A) and a 1000-to-1 on-PCB attenuator (plotted as VIN in Fig. 17) to set the amplitude of the neural signal before amplification. LED_FIRE in the second row of Fig. 17 is the chip internal signal that triggers the firing of the PGM LED packets (Fig. 9); the time interval between adjacent packets was inversely proportional to the average SBP. In other words, when there is active neural activity, the LED packets are fired more frequently. The internal LED_FIRE signal was measured through the digital monitoring buffer as a baseline to validate the wirelessly measured uplink signal. The SPAD Output (the third row in Fig. 17) is the measured photon detection result from the SPAD detector including true photon counts received

from the actual LED and the intrinsic dark counts (Fig. 17) Using the 16b-PGM LED pattern, the wirelessly measured SPAD Output was matched filtered in MATLAB, and the decoded LED_EN in the last row in Fig. 17 matched exactly with the baseline (LED_FIRE), successfully rejecting the dark counts.

C. In-vivo Measurement

All procedures complied with the guidelines of the University of Michigan's Institutional Animal Care and Use Committee. The AFE functionality was verified *in vivo* using a carbon fiber inserted into the motor cortex of an anesthetized Long Evans rat (Fig. 18(a) and (b)). A bare carbon fiber (d= 6.8μm was mounted on a daughter PCB using silver epoxy. The fiber was then Parylene C coated (t=800nm), the tip re-exposed, and coated with PEDOT:pTS to lower the impedance. The inserted carbon fiber was electrically connected to the input (VIN in Fig. 18(b)) of the proposed chip on a motherboard and a commercial high-power neural recording system (RA 16AC headstage, RA16PA pre-amp and RX7 stimulator base station, TDT Inc.) simultaneously. A bone screw, serving as ground for both recording systems, was placed at the most posterior portion of the skull and was also electrically connected to the proposed IC and the commercial recording system in parallel (REF in Fig. 18 (b)). The proposed SBP was decoded from the time interval of the measured LED_EN signal, while the conventional SBP was calculated in MATLAB using the raw data acquired by the commercial recording system (high-pass filtered at 2.2Hz by the headstage, anti-aliased filtered at 7.5kHz, and sampled at 24.414kHz). The SBP acquired using the proposed IC achieved a correlation coefficient of 0.797 to the conventional SBP.

D. Motor Prediction with the Pre-recorded Neural Signal

The one-dimensional finger position and velocity of a monkey was predicted using a 20-channel prerecorded motor cortex signal and the resulting SBP from the IC with both fixed gain and off-chip RGC (Fig. 19). A Kalman filter (KF) was used for training and prediction [21-23]. The first 100s of the measured SBP and prerecorded finger movement was used for training, and the next 24s of the finger movement was predicted with the trained KF and the measured SBP. In Fig. 19, three predicted finger positions are compared with the actual finger movement. The conventional SBP was obtained from bandpass filtering and absolute averaging on the raw prerecorded neural signal measured from a high-power analog front end in MATLAB [21-23]. The proposed SBP measured by the chip successfully predicts the finger position / velocity with a correlation coefficient of 0.864 / 0.492 with a fixed gain configuration across 20 channels, indicating only small accuracy degradation compared to the high-power conventional SBP method achieving 0.889 / 0.616 (Fig.19(c)). With the RGC, the gain configuration of each channel case was updated to optimize the average LED firing rate by increasing the gain for the channel case when the average LED firing rate was too low, and vice versa (Fig 19(b)). With the off-chip RCG, the proposed SBP achieved a prediction correlation coefficient of 0.870 / 0.569 (Fig 19(c)), and the LED firing rate remained below 50Hz across all the channels, allowing for increased channel utilization.

V. Conclusion

This article proposes a light-tolerant wireless neural recording IC for motor prediction with NIR-based power and data telemetry, addressing a unique challenge of light-robust low-power circuit design. The proposed IC can fully function under 300μW/mm^2 of light exposure, thanks to its R_{PSD}-less AFE design and novel digital SBP extractor, whereas other state-of-the -art optical-based standalone recorders [15,16] do not consider light tolerance in their designs. The proposed recorder achieves the lowest power consumption of 0.57μW at 38°C with 4.1 noise efficiency factor (NEF) with an active area of 0.19 × 0.28mm (Table III). The IC supports optical powering and bi-directional data telemetry along with a vertical stacked dual junction PV and LED GaAs chip [19]. 11pF of on-chip MIM decoupling capacitors and 27pF of intrinsic PV cell capacitance minimize random fluctuation of V_{DD} while AFE achieves high PSRR above 6 7dB to prevent power supply noise coupling. SBP, the neural feature of interest, is on-chip extracted and fired out to a repeater through the custom LED with PGM-SIM uplink signal. The data downlink is performed by PWM optical modulation while sufficient hysteresis voltage (V_{IH}-V_{IL}, 91mV, simulated) of the ORx and hardwired passcode in CDR prevents false trigger and false data downlink from random V_{DD} fluctuation. In addition, the RGC capability with the individual mote downlink provides the potential for future systematic optimization (i.e., off-chip automatic gain control) of the channel utilization and decoding accuracy when multiple motes are implanted. We expect full integration of the implantable floating mote with the proposed IC and other components in the future, enabling true wireless long-term neural recording with minimum risk of brain tissue damage.

Acknowledgement

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Biography

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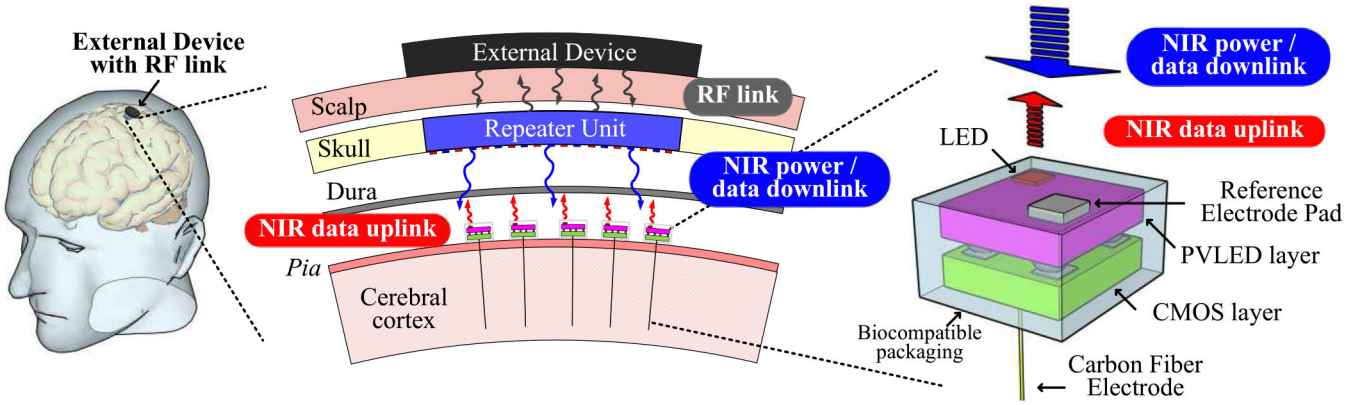


Fig. 1.

Conceptual illustration of two-step wireless neural recording system and NIR based free-floating motes.

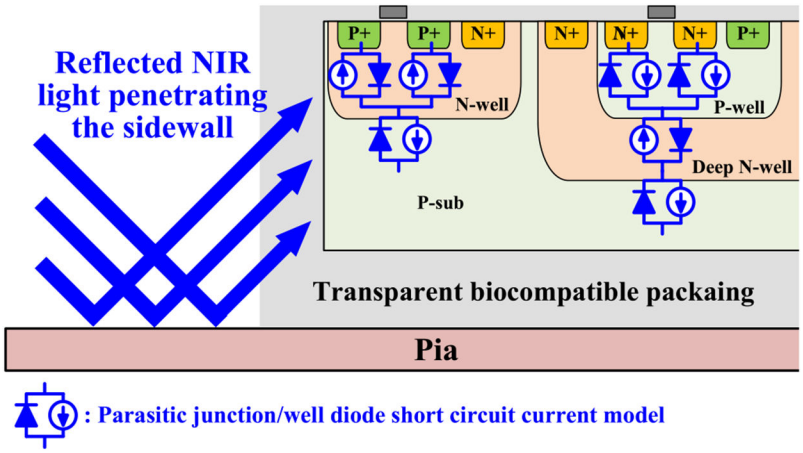


Fig. 2.
Cross section of the CMOS circuit layer with light-induced parasitic short circuit currents.

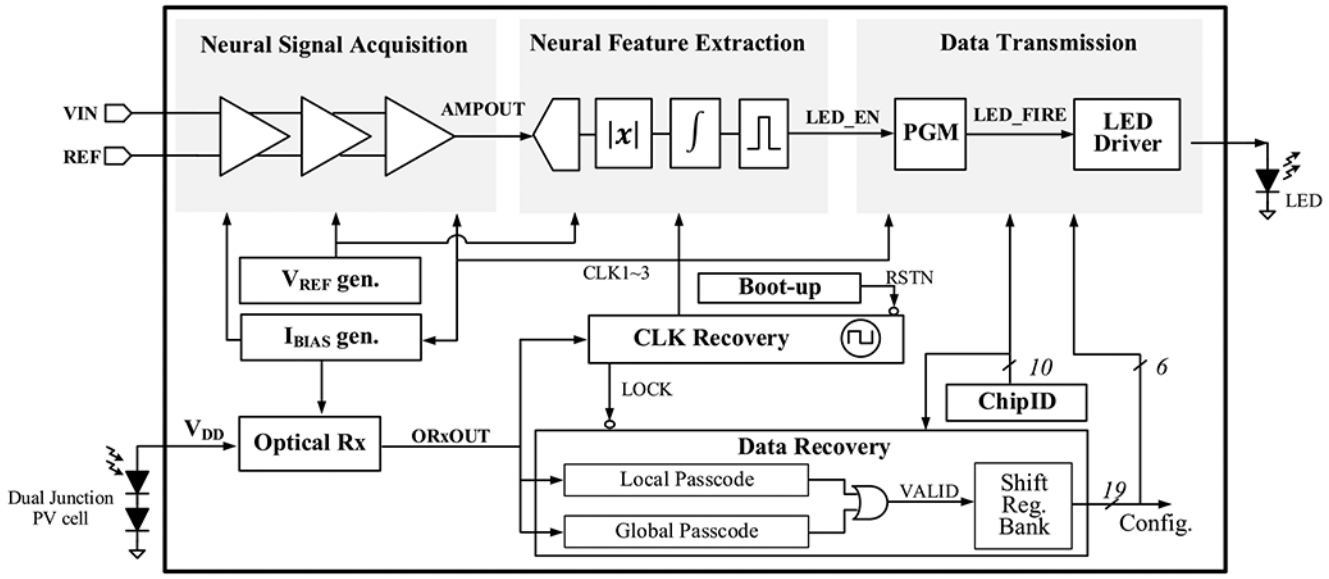


Fig. 3.
Top circuit diagram of the proposed light tolerant neural recorder.

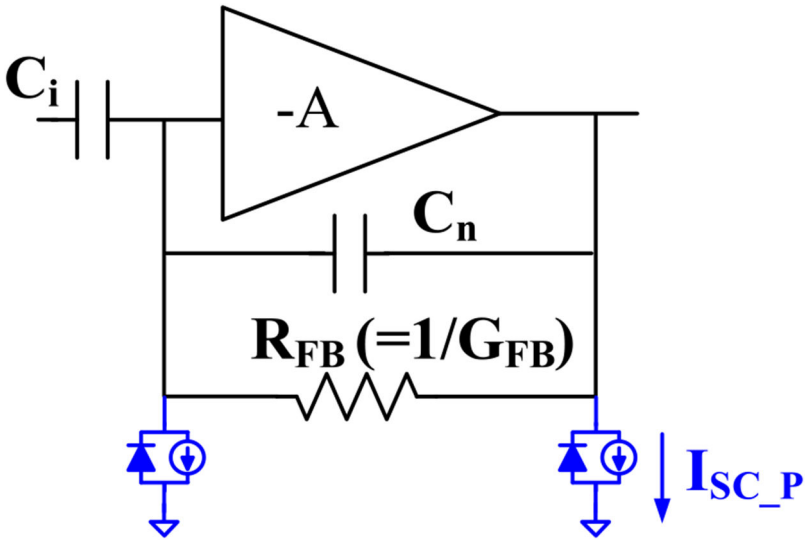


Fig. 4.

Capacitive amplifier with the feedback resistor R_{FB} and parasitic light-induced short circuit current I_{SC_P}.

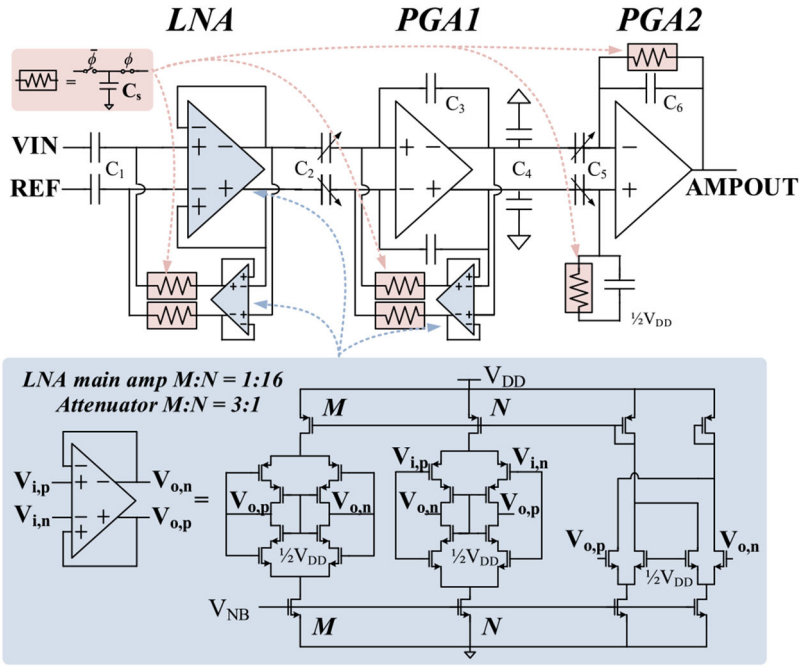


Fig. 5.
Proposed light robust neural amplifier chain.

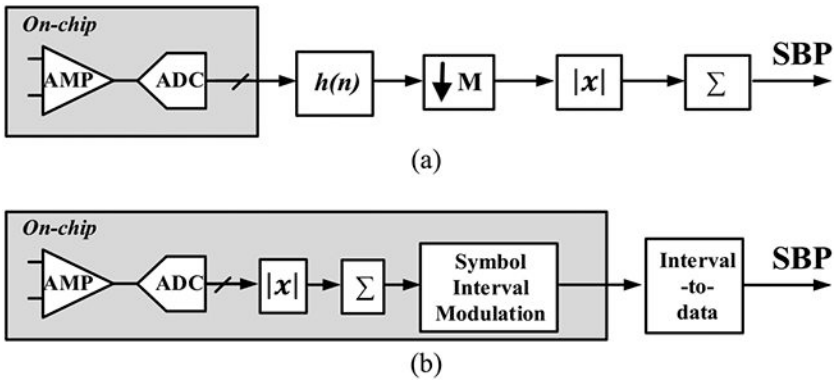
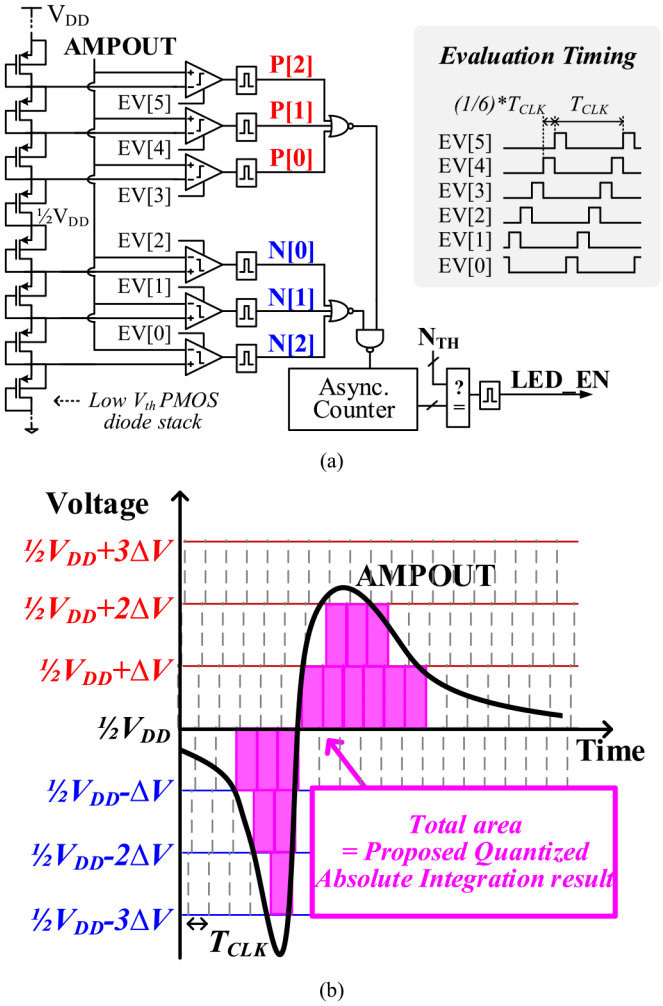


Fig. 6.
(a) Conventional approach of extracting SBP (b) proposed approach of extracting SBP.



(a)

(b)

Fig. 7.

(a) Proposed SBP extraction unit and (b) quantization of absolute amplitude and width from the SBP extraction unit.

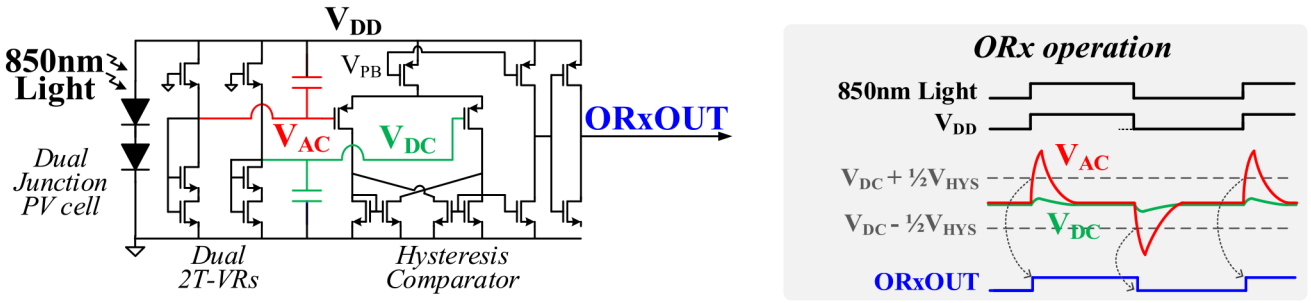


Fig. 8.
The proposed dual 2T-VRs and hysteresis comparator based ORx.

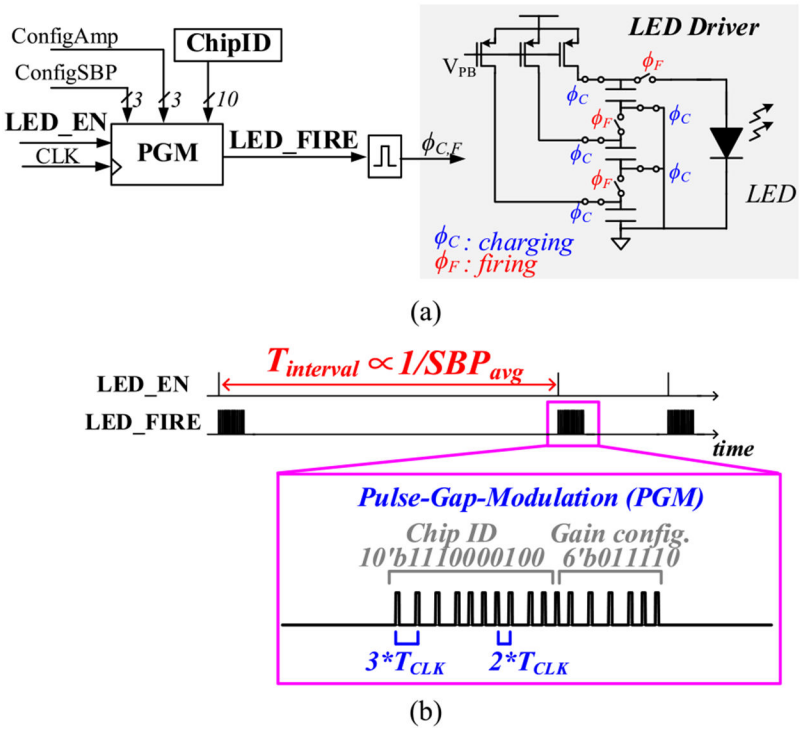


Fig. 9.

(a) Proposed PGM and LED driver and (b) Symbol-interval-modulation (SIM) and pulse gap modulation (PGM)

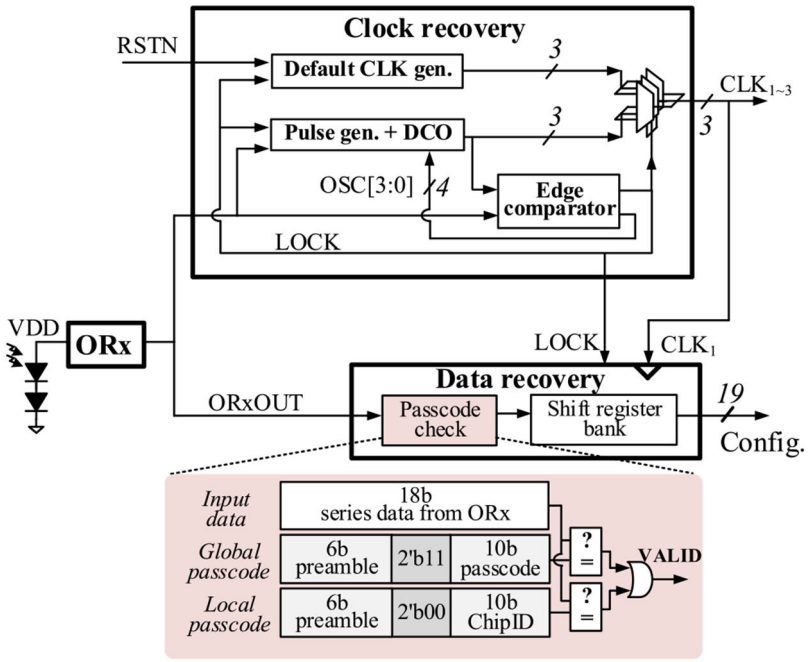


Fig. 10.
Proposed clock and data recovery (CDR) block

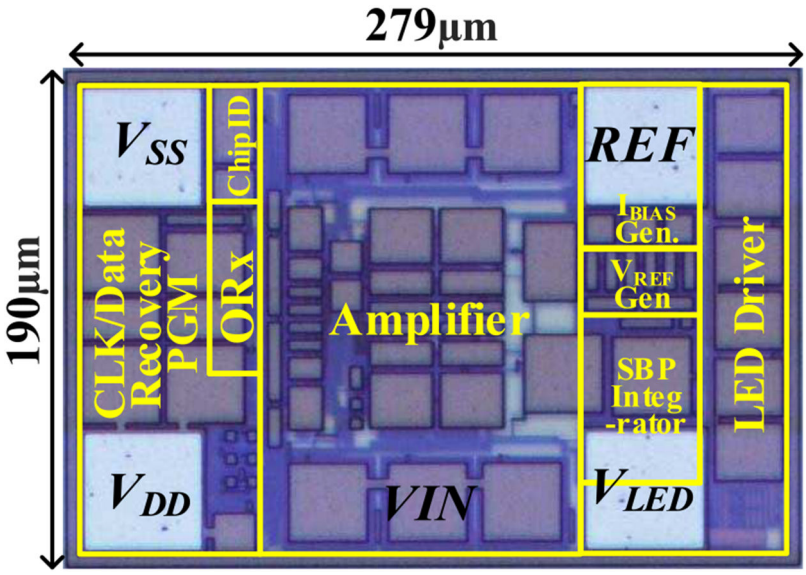


Fig. 11.
Die photo.

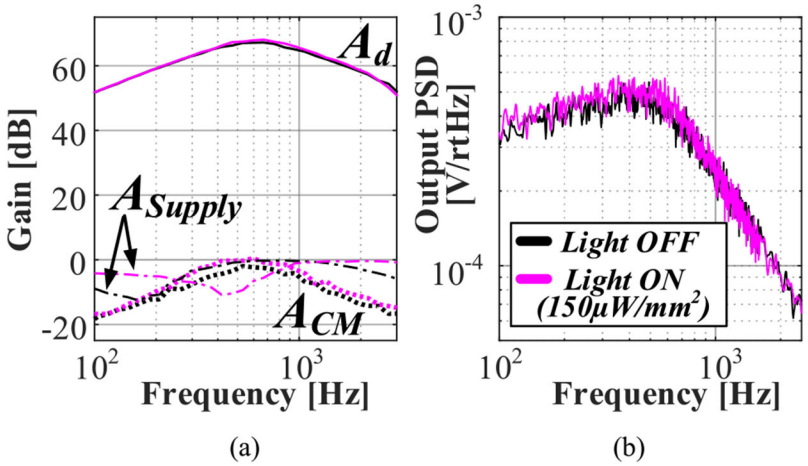


Fig. 12.

(a) Measured amplifier AC performance and (b) output noise power spectral density

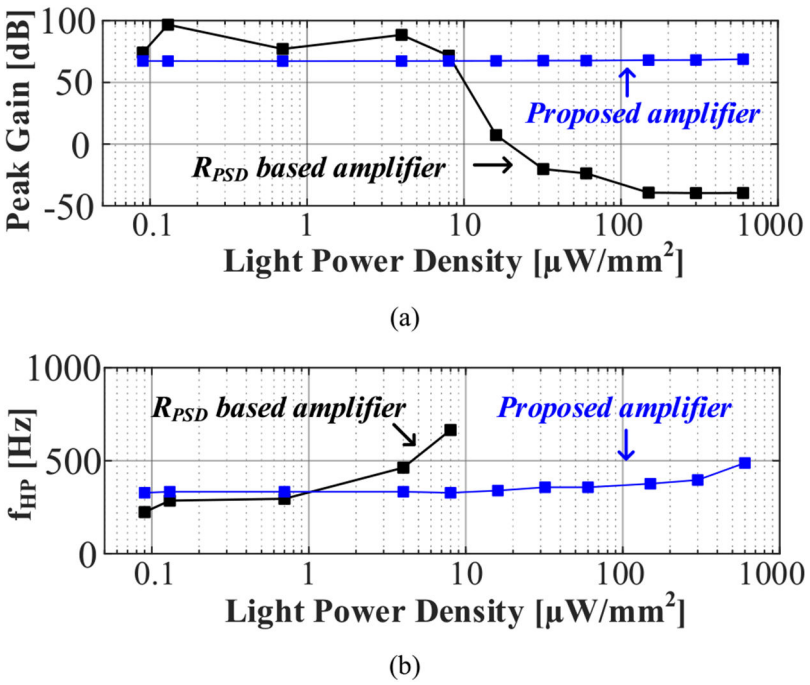


Fig. 13.

(a) Measured peak gain and (b) high pass corner sweeping NIR light intensity.

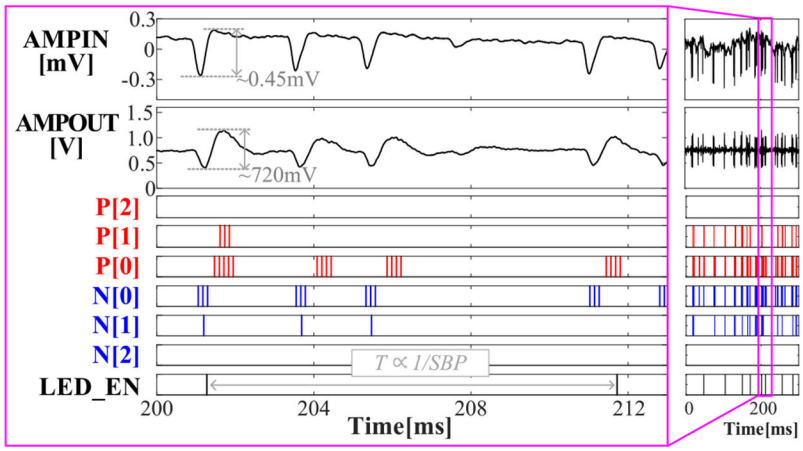


Fig. 14.

Measured transient waveform of the SBP extraction unit under 300μW/mm^2 NIR light.

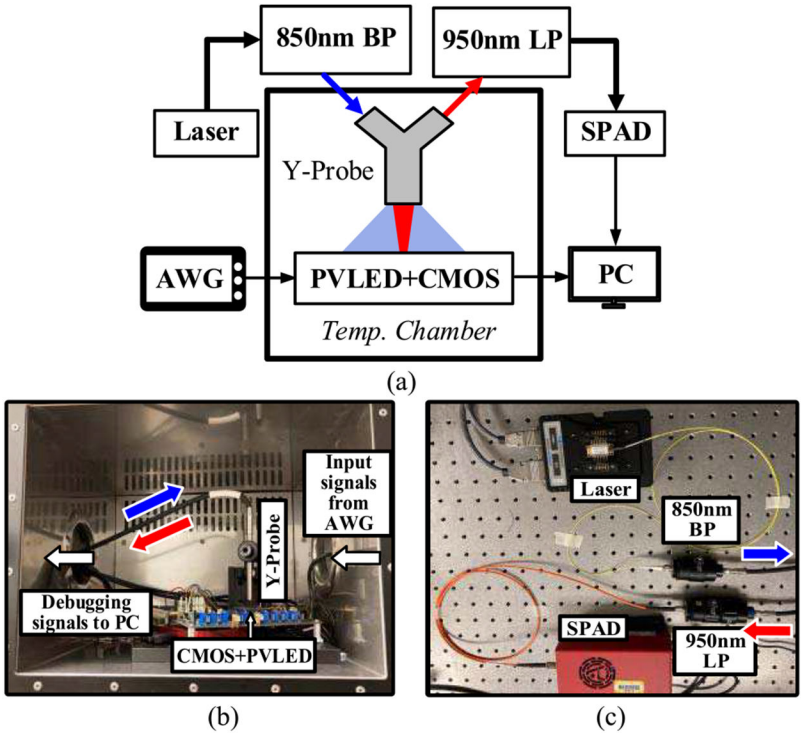


Fig. 15.

(a) Wireless optical setup diagram, (b) side view photo of the wireless optical setup inside temperature chamber, and (c) top view photo of the external light source and SPAD.

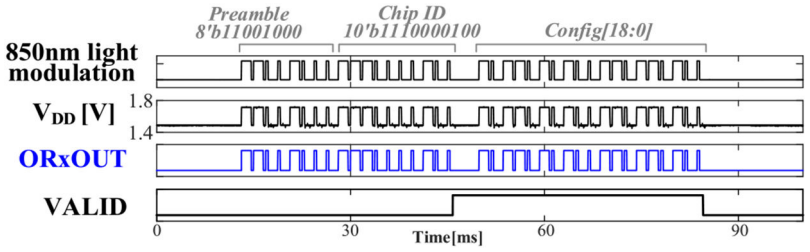


Fig. 16.
Measured local programming with the fully wireless optical setup.

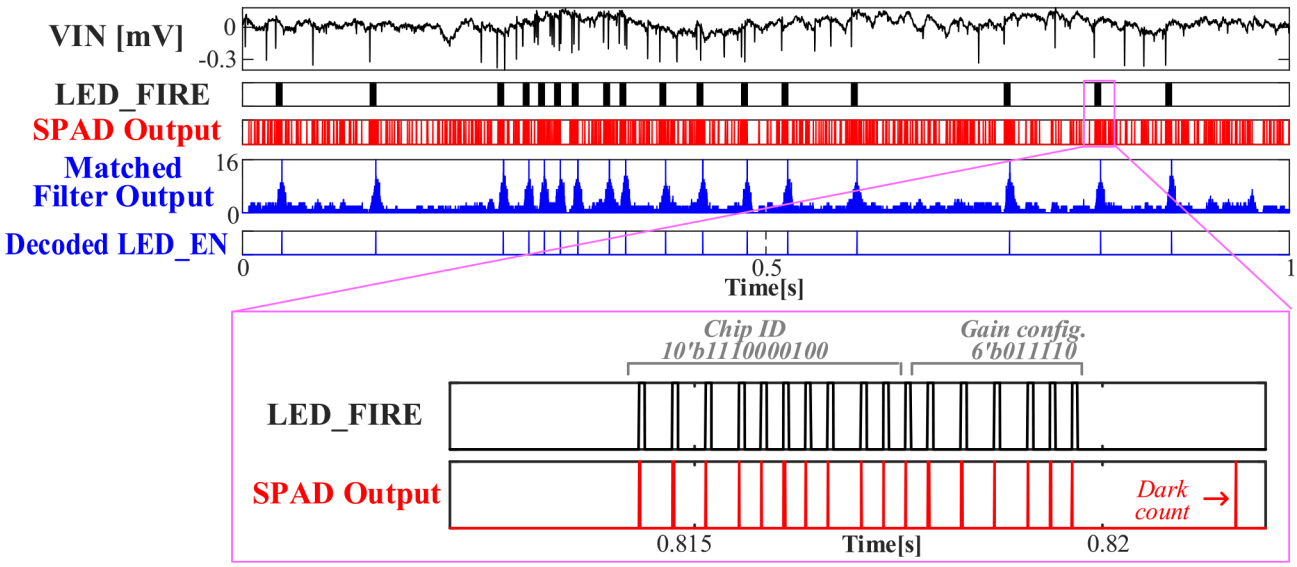


Fig. 17.
Measured data uplink with the fully wireless optical setup.

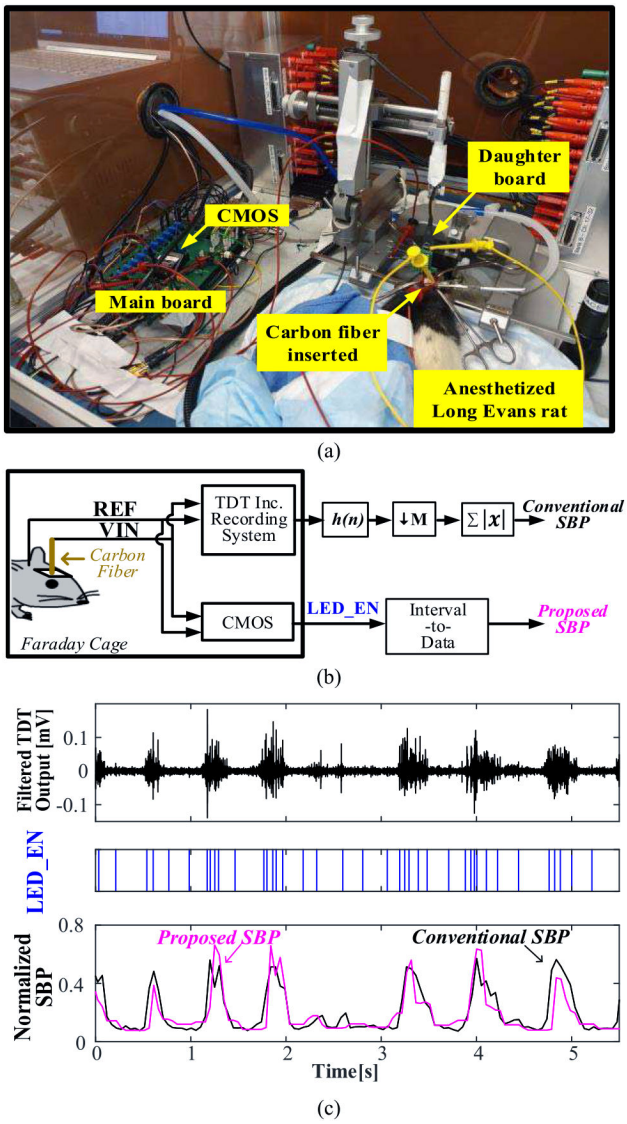


Fig. 18.

(a) *in vivo* measurement setup photo, (b) setup diagram, and (c) measured transient waveform.

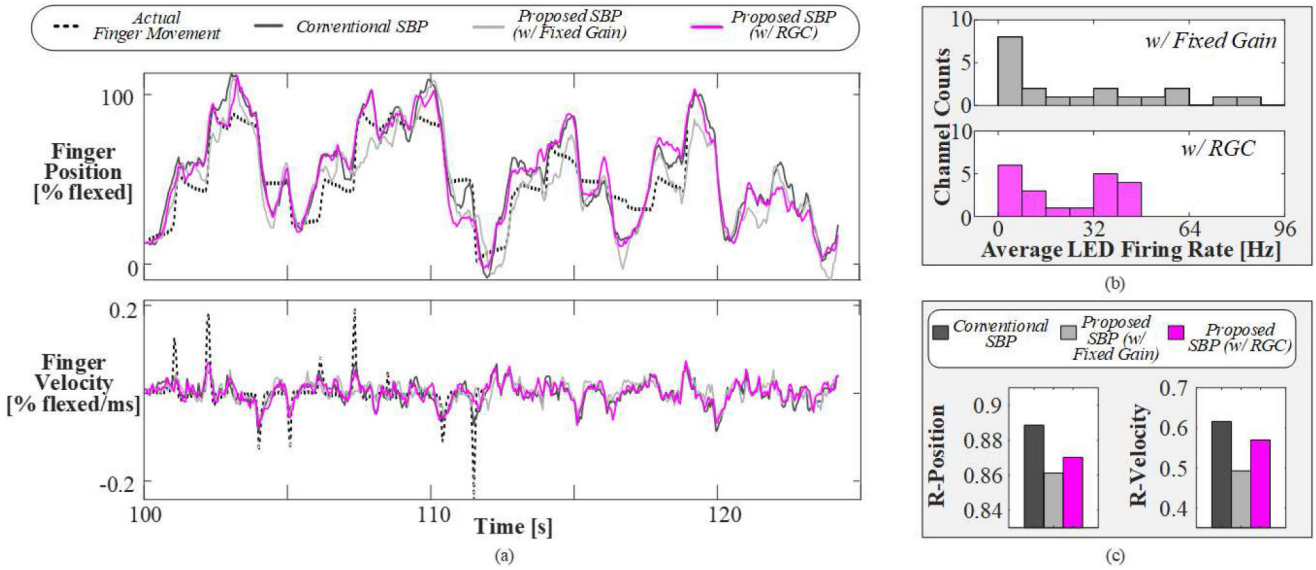


Fig. 19.

Finger movement decoding result (a) predicted finger position and velocity, (b) average LED firing rate histogram, and (c) position and velocity prediction accuracy.

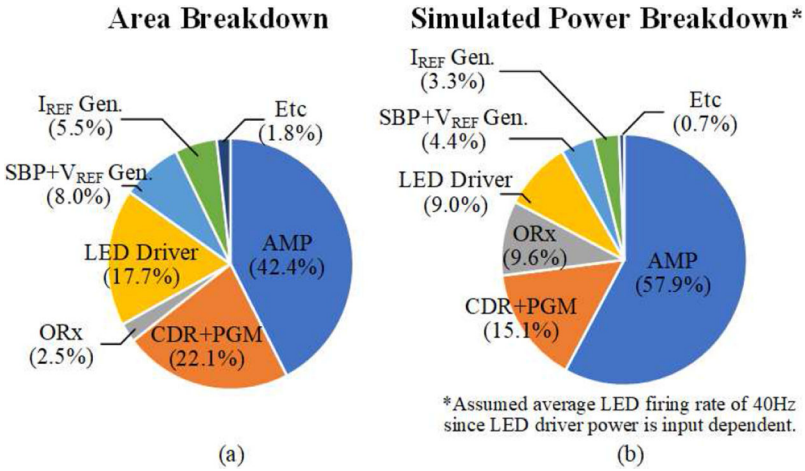
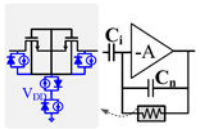
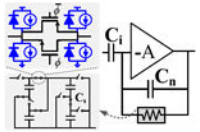
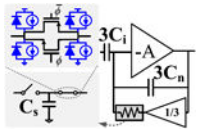


Fig. 20.
(a) Area and (b) simulated power breakdown.

TABLE I

Simulated Light Robustness of Three Different Feedback Resistors

R_{FB} Type	R_{PSD}	Series-to-parallel *Cs* [27]	Attenuator + C_s
Structure			
f_{HP}	$(\frac{1}{2\pi})(\frac{1}{R_{PSD}C_n})$	$\left(\frac{1}{20\pi}\right)\left(\frac{C_S}{C_n}\right)f_{clk}$	$\left(\frac{1}{18\pi}\right)\left(\frac{C_S}{C_n}\right)f_{clk}$
G_{FB} [pS]	0.16	9.1	117.3
I_{SC_P} [pA]	1375	63	18
$a_{LR}(=G_{FB}/I_{SC\_P})$ [V^{-1}]	0.00012	0.14	6.52

* I_{SC_P} proportional to junction area is modeled in simulation

** Simulation parameters: R_{PSD} = 6.3TΩ, C_S = 11fF, f_{CLK} = 8kHz, each junction-to-well area = 0.25μm^2, p-well-to-deep-n-well area of R_{PSD} = 15μm^2

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TABLE II

Measured amplifier AC performance

	Light OFF	**Light ON (150μW/mm^2)**
Peak Gain [dB]	67.2	68.0
CMRR [dB]	69.7	72.2
PSRR [dB]	67.5	69.2
BW [Hz]	[350, 1080]	[380, 1060]
ORN [mV_{RMS}]	12.7	13.5
IRN [μV_{RMS}]	6.2	6.2

* Measured in 38°C

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TABLE III

Comparison Table

		This work	ISSCC 2020 [16]	TBioCAS 2018 [15]	NER 2019 [13]	JSSC 2019 [14]
Technology [nm]		**180**	180	180	65	65
Wireless Method		**Optical**	Optical	Optical	RF	Ultrasonic
	Area [mm^2] (W[mm] × L[mm])	**0.053 (0.19 × 0.28)**	0.032 (0.19 × 0.17)	0.014 (0.25 × 0.06)	0.250 (0.50 × 0.50)	0.250 (0.50 × 0.50)
Data Link	Uplink	**PGM-SIM**	Manchester-SIM	PPM	RF	AM
	Downlink	**PWM**	PWM	No	ASK-PWM	No
	Mote-Level Gain Control	**Yes**	No	No	No	No
On-chip Feature Extraction		**SBP (digital)**	SBP (analog)	No	No	No
Chip ID		**Yes**	Yes	No	Yes	Yes
Clock Recovery		**Yes**	Yes	No	No	No
Use of Pseudo Resistor		**No**	Yes	Yes	No	No
Light Tolerant Design (max. light power density)		**Yes (300μW/mm^2)**	No	No	N/A **	N/A **
Supply [V]		**1.55**	1.5	0.9	0.6	1
Power	Total [μW]	**0.57** †	0.74 †	1	40	28.8
	Amplifier [μW]	**0.36** †	0.51 †	0.5	3.2	4
Target neural signal		**AP**	AP	LFP, AP	ECoG	LFP, AP
Gain [dB]		**67.2** †	69.0 †	30.0	N/A	24.0
Bandwidth [Hz]		**[350, 1080]** †	[180, 950] †	10000	500	5000
CMRR [dB]		**69.7**	N/A *	N/A *	N/A *	N/A *
PSRR [dB]		**67.5**	N/A *	N/A *	N/A *	N/A *
IRN [μV_{RMS}]		**6.2** †	4.8 †	15	2.2	5.9
NEF		**4.10** †	3.76 †	4.31	8.70	5.87

† Measured at 38°C

* Not Available

** Not Applicable