KASLR is Dead: Long Live KASLR

D. Gruss, M. Lipp, M. Schwarz, R. Fellner, C. Maurice, S. Mangard

July 5, 2017—ESSoS'17

Graz University of Technology

Motivation

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  - In Software?

Background

Virtual Memory

- Maps virtual addresses used by a program to physical addresses in DRAM

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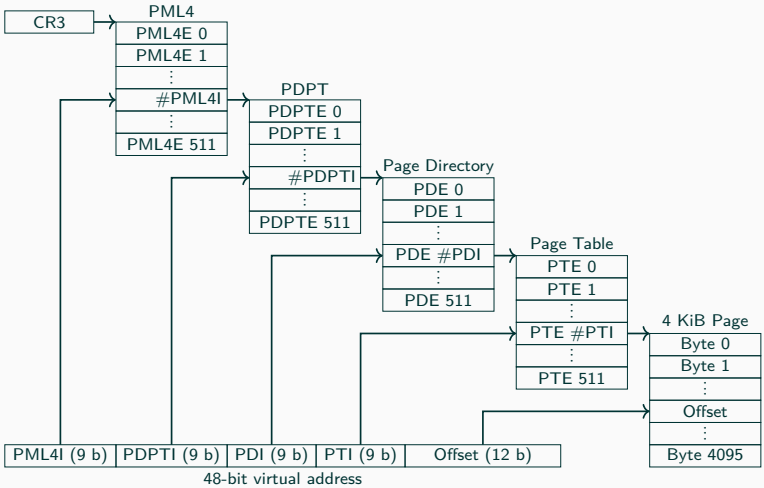
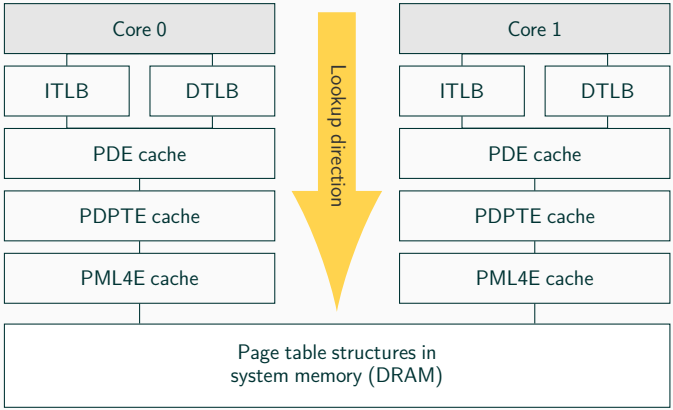
- Virtual address space is organized in pages
- Page tables are used to translate virtual to physical addresses

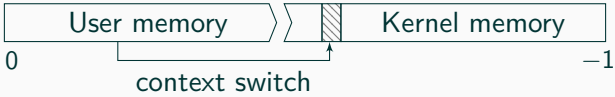
Address Translation on x86-64



Address Translation Caches



Address Space



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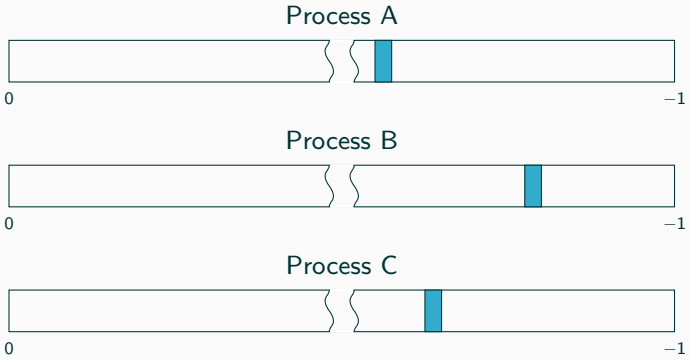
- Statistical mitigation of memory corruption vulnerabilities
- Randomizing core kernel image and device drivers position at boot time
- Enabled in Linux 4.12 by default (May 2017)



- Driver is loaded to a different offset on every boot

Attacks against KASLR

TSX Attack

- 2016 by Jang et al. [Jan+16]
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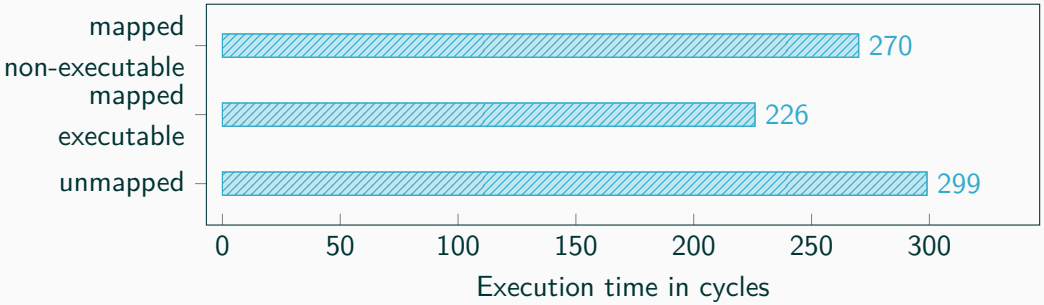
- Reveal mapping status of each page
- Detect kernel modules with unique size signature
- Less noisy than Double Page Fault Attack by Hund et al. [Hun+13]


mapped
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Execution time in cycles

Prefetch Side-Channel Attack

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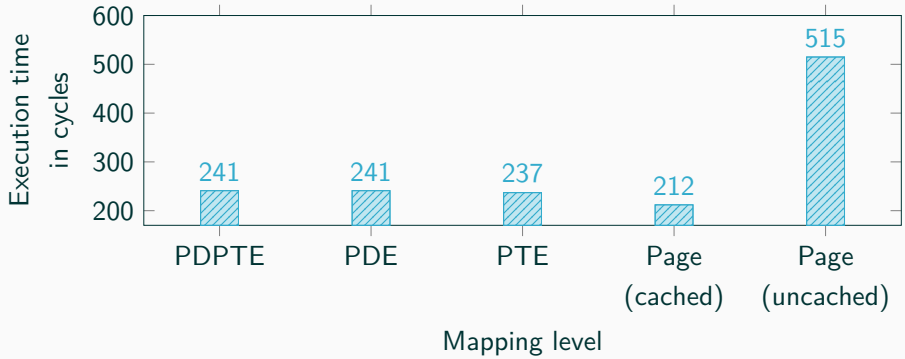
- Reveal mapping status
- Allows to obtain physical address of virtual address


Execution time in cycles
600
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241
237
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515
PDPTE
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Page (cached)
Page (uncached)
Mapping level

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Idea

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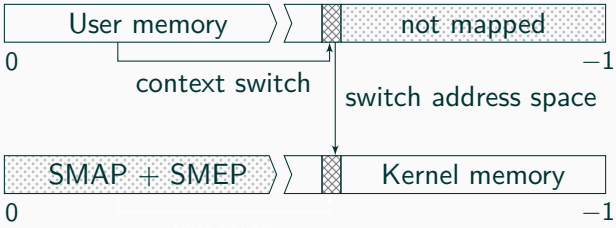
- Kernel Address Isolation: Separate kernel space and user space



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- **Challenge 2:** Several locations must be valid for both user space and kernel space during context switches. Identify them.
- **Challenge 3:** Switching the address space incurs an implicit TLB flush. Performance impact.

Solving Challenge 1

- Every process has two address spaces:

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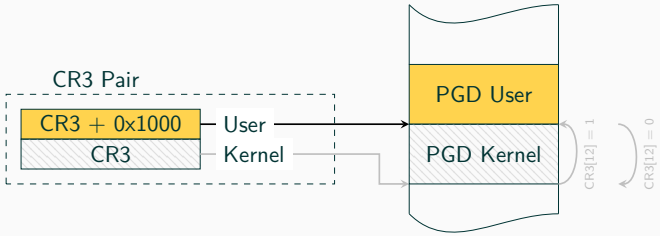
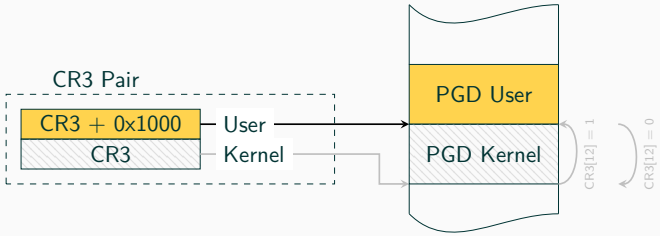
- Switching between the address space:
  - Update CR3 with corresponding PML4



- Power-of-two offset between kernel and shadow PML4



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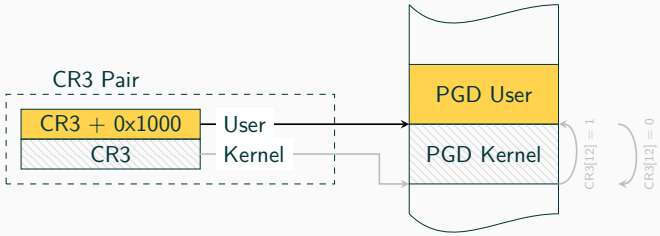

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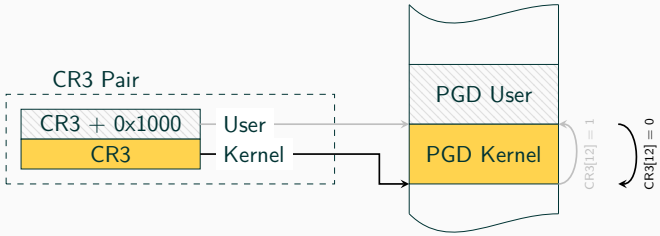

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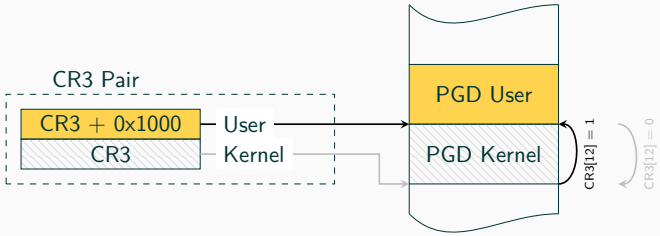

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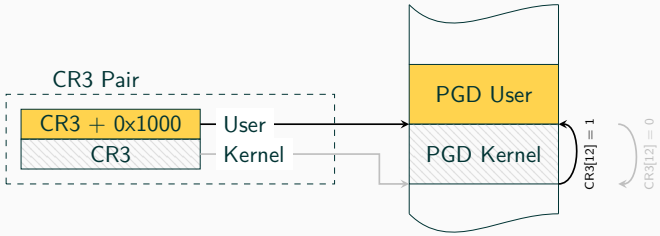

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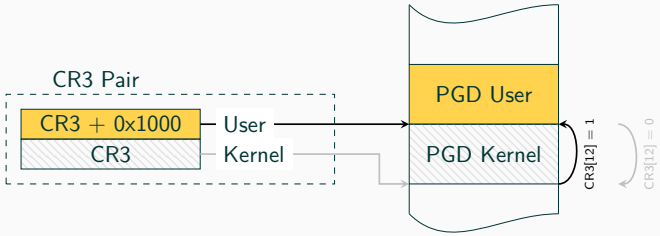

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- 8kb-aligned physical memory block to store both PML4s
- Toggle bit 12 of the physical address to switch between mappings
- No memory lookups
- Only a single scratch register

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- Not practical
  - In reality, much more has to be mapped

Solving Challenge 2

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- Multi-threaded applications running on different cores:
  - per-CPU memory regions
  - interrupt request (IRQ) stack and vector
  - global descriptor table (GDT)
  - task state segment (TSS)
  - thread stacks

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- SMEP: Protects against executing user space code from kernel mode
- SMAP: Invalid user memory references in kernel mode

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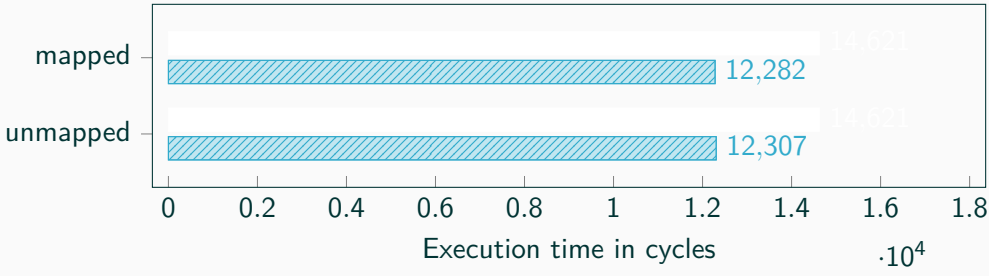
- Tag TLB with CR3 [Ven+12]

Evaluation

Double Page Fault Attack



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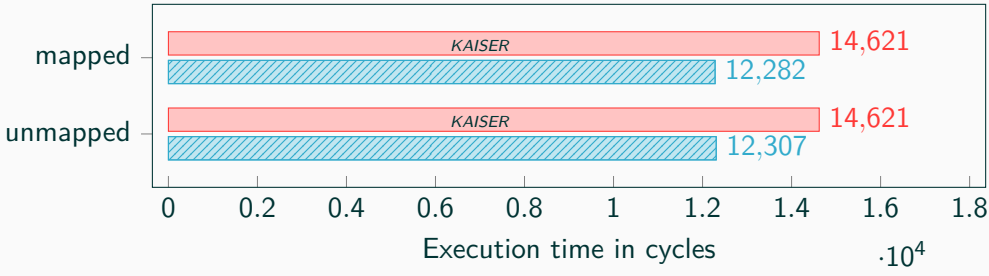

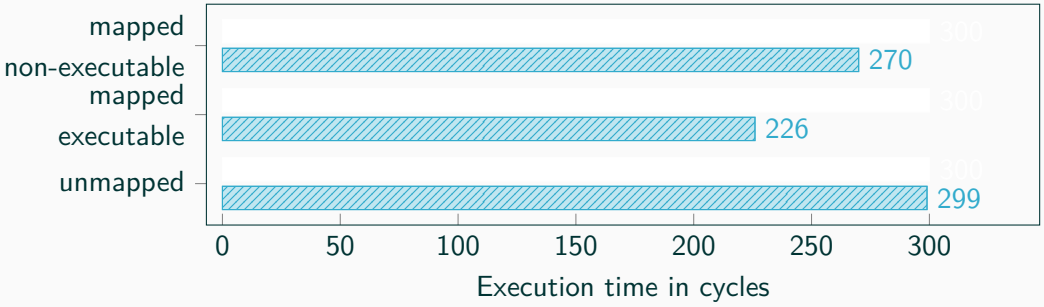
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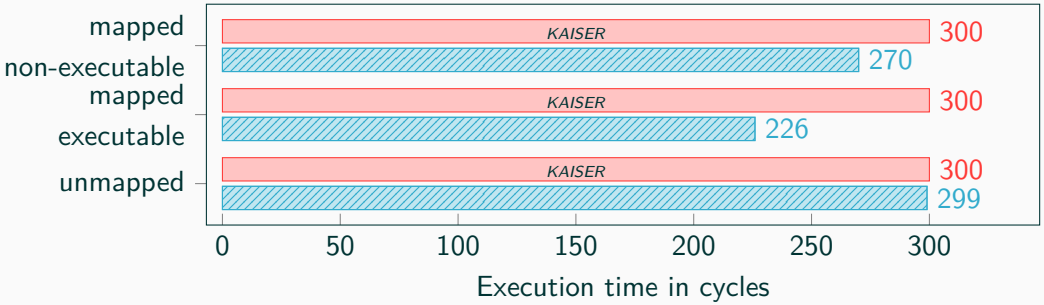
Execution time in cycles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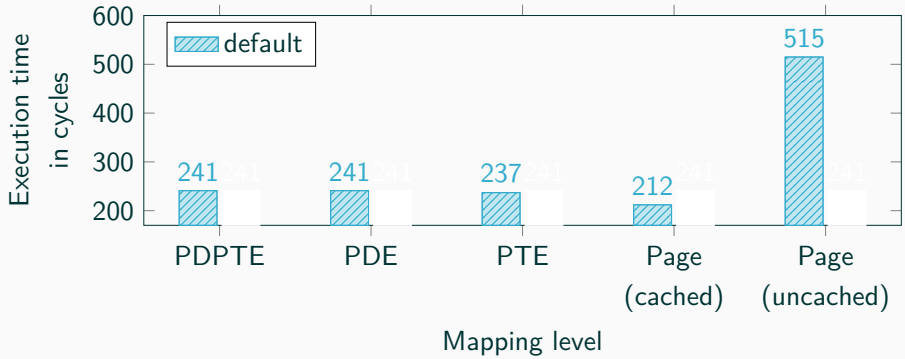
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600
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default
241
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237
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PDPTE
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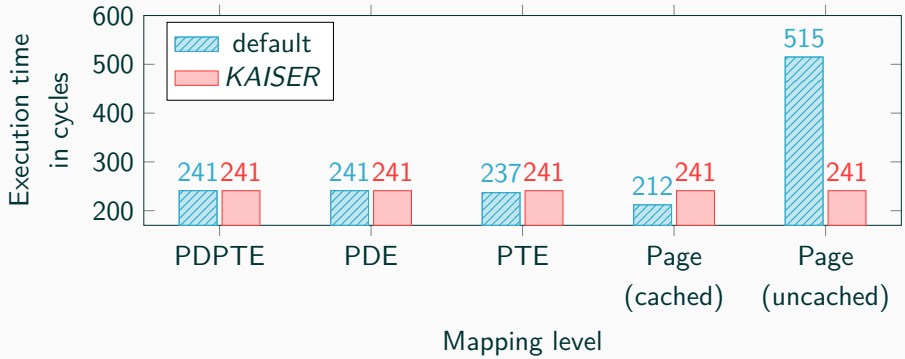
Page (cached)
Page (uncached)
Mapping level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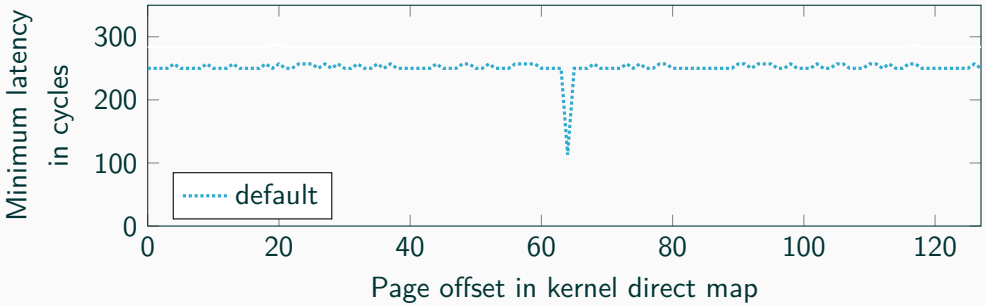
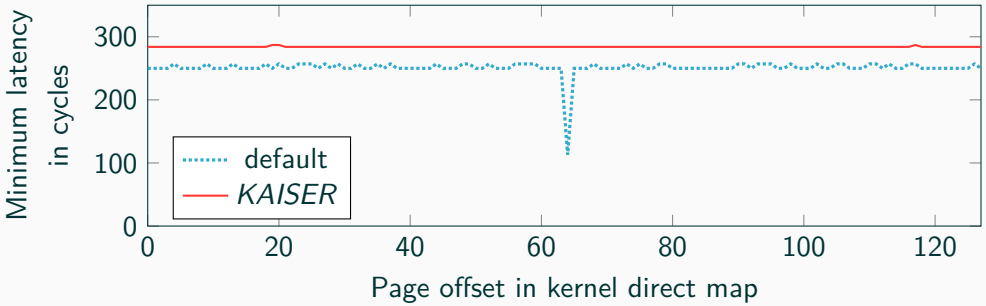

Minimum latency
in cycles
300
200
100
0
default
0
20
40
60
80
100
120
Page offset in kernel direct map


Minimum latency
in cycles
300
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100
0
default
KAISER
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120
Page offset in kernel direct map

Performance

Benchmark	Kernel	Runtime				Average Overhead
		1 core	*2 cores*	*4 cores*	*8 cores*	
PARSEC 3.0	default	27:56,0 s	14:56,3 s	8:35,6 s	7:05,1 s	0.37 %
	KAISER	28:00,2 s	14:58,9 s	8:36,9 s	7:08,0 s	
pgbench	default	3:22,3 s	3:21,9 s	3:21,7 s	3:53,5 s	0.39 %
	KAISER	3:23,4 s	3:22,5 s	3:22,3 s	3:54,7 s	
SPLASH-2X	default	17:38,4 s	10:47,7 s	7:10,4 s	6:05,3 s	0.09 %
	KAISER	17:42,6 s	10:48,5 s	7:10,8 s	6:05,7 s	

Github

Source available on Github:

https://github.com/iaik/kaiser

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- KAISER prevents existing side-channel attacks
  - Double Page Fault Attacks
  - TSX-based side-channel attacks
  - Prefetch side-channel attacks
- Minor performance overhead on modern commodity hardware

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