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Authors

Kleinfelder, S.A.
Levi, M.
Milgrome, O.

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Lawrence Berkeley Laboratory
UNIVERSITY OF CALIFORNIA

Physics Division

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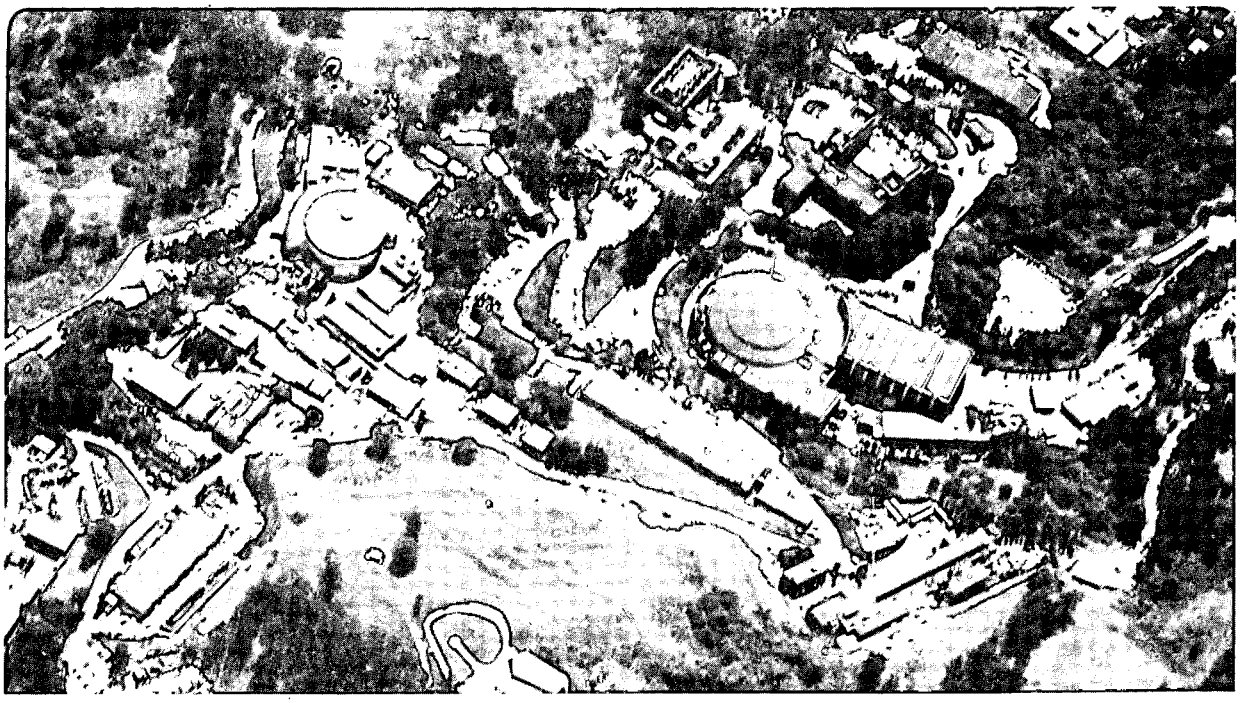

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TEST RESULTS OF A 90 MHZ INTEGRATED CIRCUIT SIXTEEN CHANNEL ANALOG PIPELINE FOR SSC DETECTOR CALORIMETRY

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Stuart A. Kleinfelder, Michael Levi, and Oren Milgrome

Physics Division
Lawrence Berkeley Laboratory
University of California
Berkeley, California 94720

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Stuart Kleinfelder, Michael Levi, Oren Milgrome
Lawrence Berkeley Laboratory*
1 Cyclotron Road
Berkeley, CA 94720

Abstract

A sixteen channel analog transient recorder with 128 cells per channel has been fabricated as an integrated circuit and tested at speeds of up to 90 MHz. The circuit uses a switched capacitor array technology to achieve a simultaneous read and write capability and twelve bit dynamic range. The high performance of this part should satisfy the demanding electronics requirements of calorimeter detectors at the SSC. The circuit parameters and test results are presented.

Introduction

The electronics for signal detection, event selection, and data recording for an SSC detector will be one of the most sophisticated electronics systems ever built. Signal processing must be performed on one trillion analog samples per second. The general task to be accomplished is the temporary storage, followed by slower readout, of brief but high speed analog transients. Acquisition with sampling frequencies up to the beam crossing rate of 62.5 MHz are needed. Usually, a trigger decision of a 1-2 microseconds latency is made to judge the value of the stored signals. These signals are then either discarded or digitized, processed, and transferred to computer systems. Thus, these systems usually require time delay via temporary storage and time stretching of the stored signal to match the bandwidth of the data processing system.

Analog Memories For Pipelined Storage

Traditional solutions to this problem have involved the use of flash analog to digital converters (FADC's) followed by digital memory, or use of charge coupled device (CCD) delay lines. The switched capacitor approach offers lower cost, lower power and higher density while providing fast sampling speeds, wider dynamic range and a higher degree of flexibility than these traditional techniques. The high density CMOS processes used are suitable for inclusion of greater signal processing power and integrated circuits (IC's) may ultimately include on-chip preamplification, signal shaping, analog to digital conversion and sophisticated addressing schemes including sparse or selective data readout and trigger buffering and selection.

The switched capacitor array (SCA) will allow for the retention of data during trigger decision. The length of the array will provide for 128 memory cells per channel of electronics, allowing up to 2 microseconds of analog information to be stored at the SSC. Three types of analog memory cells are being pursued. One of these, a single-ended single ported analog pipeline, has been previously reported.[1] A second type, with simultaneous read-write capability has recently been fabricated, the test results from this device are reported here. A third type, with fully differential inputs is in development but will not be discussed in this report.

Circuit Description

The SCA (Switched Capacitor Array) integrated circuit uses a two micron double metal CMOS process with two layers of polysilicon forming the high density capacitors prototyped through MOSIS. It has 16 parallel analog signal inputs and 16 parallel analog outputs. Two digital clock inputs, a reset control input, and two address busses are used to operate the circuit. Fig. 1 shows the device concept. The analog memory being developed permits simultaneous read and write operations providing deadtimeless operation of the memory.

The circuit contains 2048 sample and hold cells subdivided into 16 parallel channels of 128 cells per channel. Each of the 16 channels has a dedicated analog input which is connected to a bus distributing the input signal to 128 sample and hold cells. Each sample and hold cell consists of a complementary CMOS transmission gate (complementary switch) and a 1 pF double polysilicon capacitor. The capacitors use a high quality silicon-oxide dielectric of 70 nm thickness. An externally supplied reference voltage is applied to the bottom plate of all capacitors. The voltage stored on each sample and hold capacitor then corresponds to the difference between the input signal from a given channel at the time its sample and hold switches are opened and the applied reference voltage. The reference voltage can be adjusted to shift the baseline for better level matching.

An address decoder turns on and off sample and hold switches using a "break before make" action. "Break before make" insures that no charge sharing between subsequently engaged capacitors can occur. During the readout sequence each sample capacitor is placed in the feedback path of the reconstruction op-amp. There is one reconstruction op-amp per channel. Before readout of each sample, stray charge on the signal distribution busses are cleared by shorting each amplifiers inverting input nodes and output nodes through a reset switch. This prevents charge remaining on parasitic nodes from the previous samples from influencing the next read out sample.

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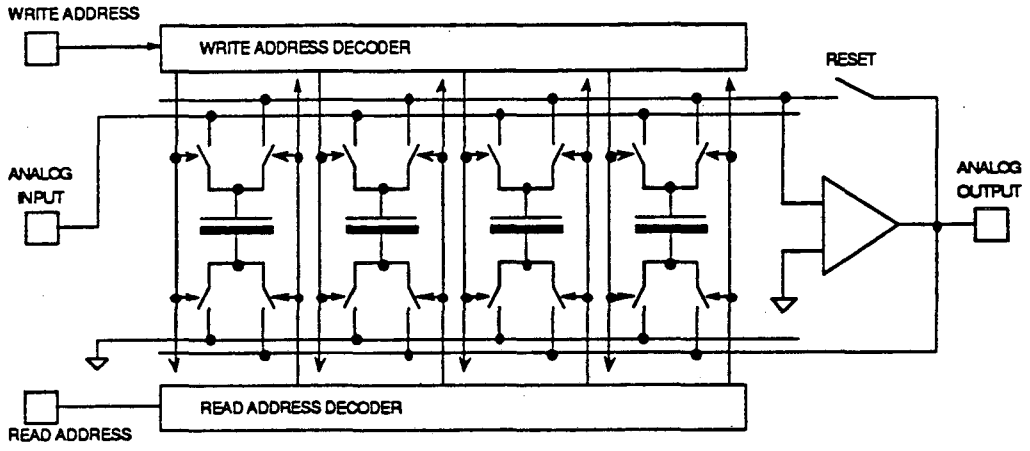

Fig. 1. A simplified block diagram of a single ended dual-ported analog memory cell structure as discussed in the text. The voltage presented at the input is stored as a charge on each capacitor in a time sequence. The selective reading and writing to and from a capacitor element is controlled by four CMOS switches. The reset switch is closed momentarily prior to each read operation. The input and output operations of the analog memory are completely separate and allow for full simultaneous read/write capability.

SCA Circuit Performance

Non-uniformities in the sample and hold elements limit dynamic range unless corrections are applied. The double polysilicon capacitors, although of excellent quality, are not likely to be uniform to better than 10 bits, but the SCA readout scheme is not sensitive to capacitor values to first order. Non-uniformity of the sample and hold switches can be important, as the charge injection from these switches (due to gate to drain capacitance) will then vary. These switches are complimentary, and therefore the charge injection is canceled to first order, but variations still exist. In addition, the rise and fall times of the clocks are very fast, and slight variations in clock skews (imperfect alignment of the complementary clocks) can also lead to imperfect cancellation.

In order to achieve 12 bit dynamic range the pedestal variation of each of the storage elements in a channel must be less than one part in 4096 of the full scale voltage range. A channel operating with a full scale range of 4 volts would then require less than 1 mV of pedestal variation per element.

To achieve 12 bit dynamic range 8.3 charging time constants must elapse in each 16 nsec write operation to charge the sample and hold capacitors, this fast input bandwidth requires a large input charging switch. For increasing switch sizes the amount of parasitic charge injection from the switch will also increase. In the version tested, with a 2 nsec charging time constant, the cell to cell pedestal variation at a 50 MHz acquisition rate was 0.4 mV rms. The cell-to-cell pedestal variation is shown for a single channel in Fig. 2.

The on-chip rail-to-rail readout operational amplifiers has been developed based on a published design.[2] The op-amp operates to within 100 mV of either voltage rail, thereby maximizing the useable dynamic range. The linearity of this op-amp, 3 mV out of a 6 volt range or 0.05%, substantially exceeds the intrinsic accuracy of any large calorimeter system under consideration. The amplifiers must drive the parasitic bottom plate capacitance of all sample capacitors (approximately 10 pF) which limits the readout rate. The overall linearity of the SCA has been limited by a layout error which will be rectified in subsequent designs.

The measured incoherent noise on any given single cell when operated with a 62.5 MHz acquisition rate is less than 0.6 mV rms. Thus, the total dynamic range (single cell) could exceed 8000:1, or 13 bits. In previous versions of the IC the clocking noise feedthrough was well below one millivolt; however, in the current version inadequate separation of the on chip digital and analog power lines have increased the clocking noise feedthrough to several millivolts. The clocking noise is absent in a differential manifestation of the IC and is expected to be absent in the next corrected version of the IC. The measured parameters of the SCA are summarized in table 1.

Table 1. Measured performance parameters of a simultaneous read-write switched capacitor array integrated circuit. Measurements were performed at a 50 MHz acquisition rate, but not utilizing the simultaneous read write capability.

Analog Store Parameters	Achieved Performance
No. channels/chip	16
No. of elements/channel	128
Power consumption/channel	23 mW
Non-linearity	+/- 0.9%
Cell to cell pedestal variation	0.3 mV rms
Charging time constant	2 ns
Channel dynamic range	4000
Maximum sample rate	90 MHz
Maximum readout rate	200 KHz
Noise floor	0.7 mV rms
Input voltage range	0.5-5.5 Volts
Capacitor droop rate	0.1 mV/msec
Output settling time (0.02%)	1.2 usec
Gain variation from unity	+/- 1.5%

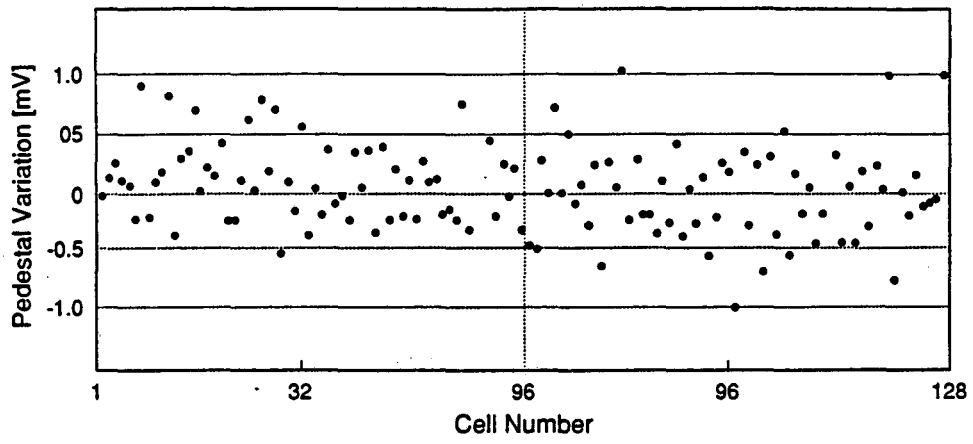

Fig. 2. Cell-to-cell pedestal variation as a function of cell number across a single channel. The small pedestal variation will permit large dynamic range operation of the circuit without corrections.

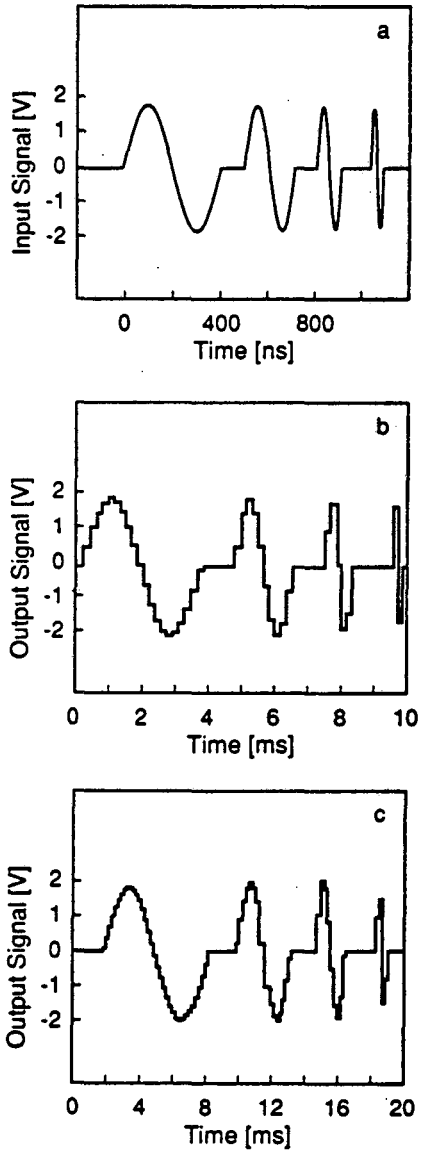

Fig. 3. In (a) is shown the input signal, 400, 200, 100, and 40 nsec period sinewaves of duration equal to the period. In (b) and (c) is shown the SCA output running at an acquisition frequency of 50 MHz and 90 MHz, respectively.

Operation of the integrated circuit has been verified on a sample of test pulses simulating the SSC calorimeter detector signals. Shown in Fig. 3 are a sequence of successively faster single cycle sinewaves, the pulses simulate the signals seen from the slowest to the fastest of the considered calorimeter detectors. Shown in (a) is the input pulse train, a 400 nsec, 200 nsec, 100 nsec and 40 nsec period sinewave. In (b) and (c) are the signals as sampled and recorded by the SCA at 50 MHz and 90 MHz acquisition rates, respectively. For illustrative purposes the readout rate has been slowed so that the comparatively short reset phase (1.6 usec) cannot be seen in these figures. The figures have been traced from AC coupled oscilloscope photographs.

Conclusions

A high accuracy analog pipeline has been implemented and is able to operate at higher speeds than those required for the SSC. Because of the low noise, pedestal variation, and rail-to-rail voltage range, 12-13 bit performance should be possible. Noise due to clock feedthrough should be corrected in the next version of the IC. At that point the chip will be fully capable of meeting the performance requirements for SSC calorimetry. Work is continuing in developing test circuits and procedures to study the chip while fully utilizing the simultaneous read-write capability of the device.

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LAWRENCE BERKELEY LABORATORY
UNIVERSITY OF CALIFORNIA
INFORMATION RESOURCES DEPARTMENT
BERKELEY, CALIFORNIA 94720